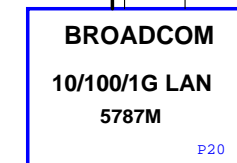
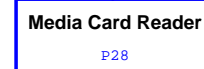
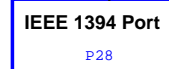
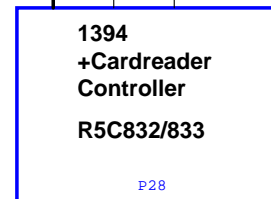
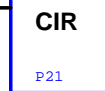
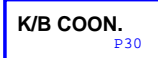
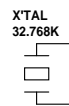
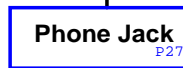
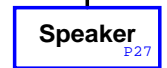
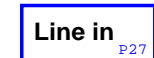
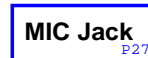
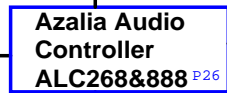
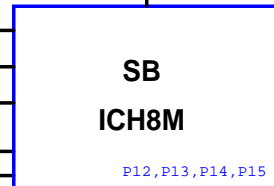
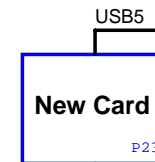
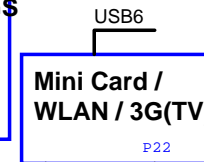
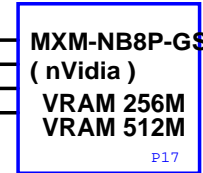
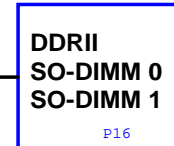
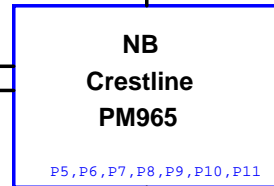
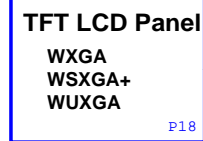
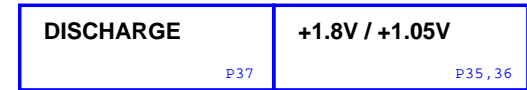
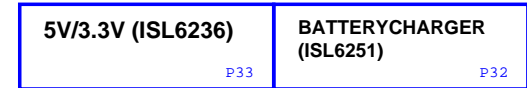
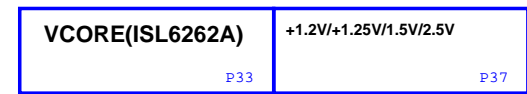
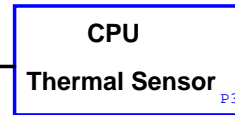
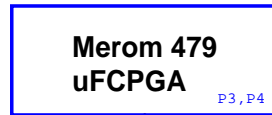
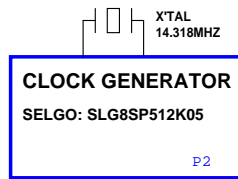
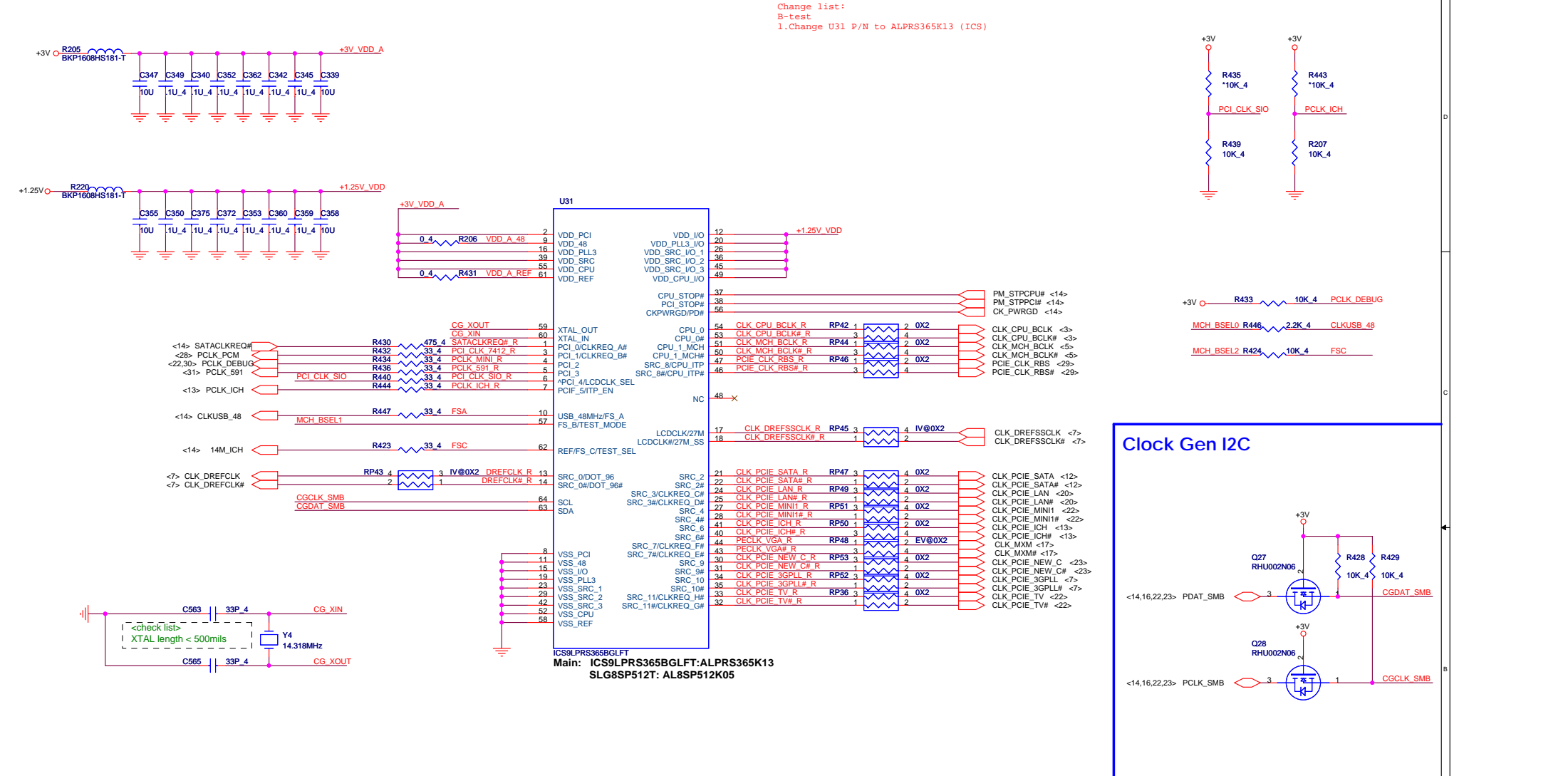


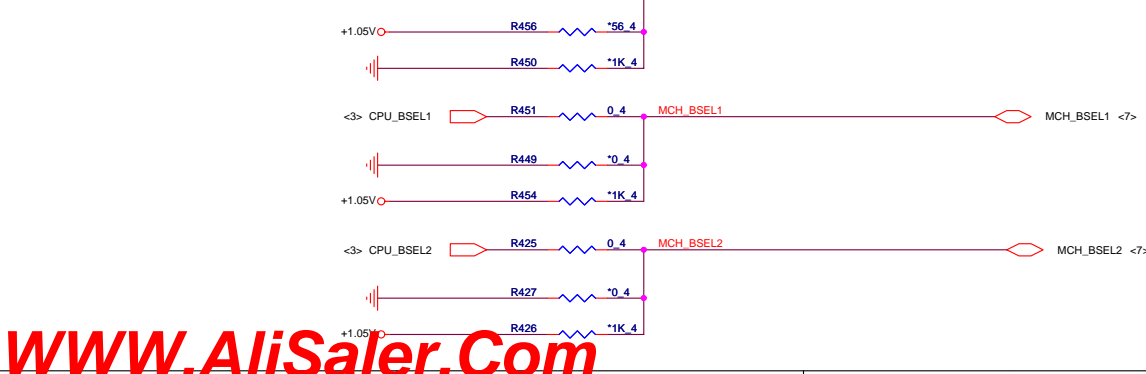
ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM



Clock Generator




CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

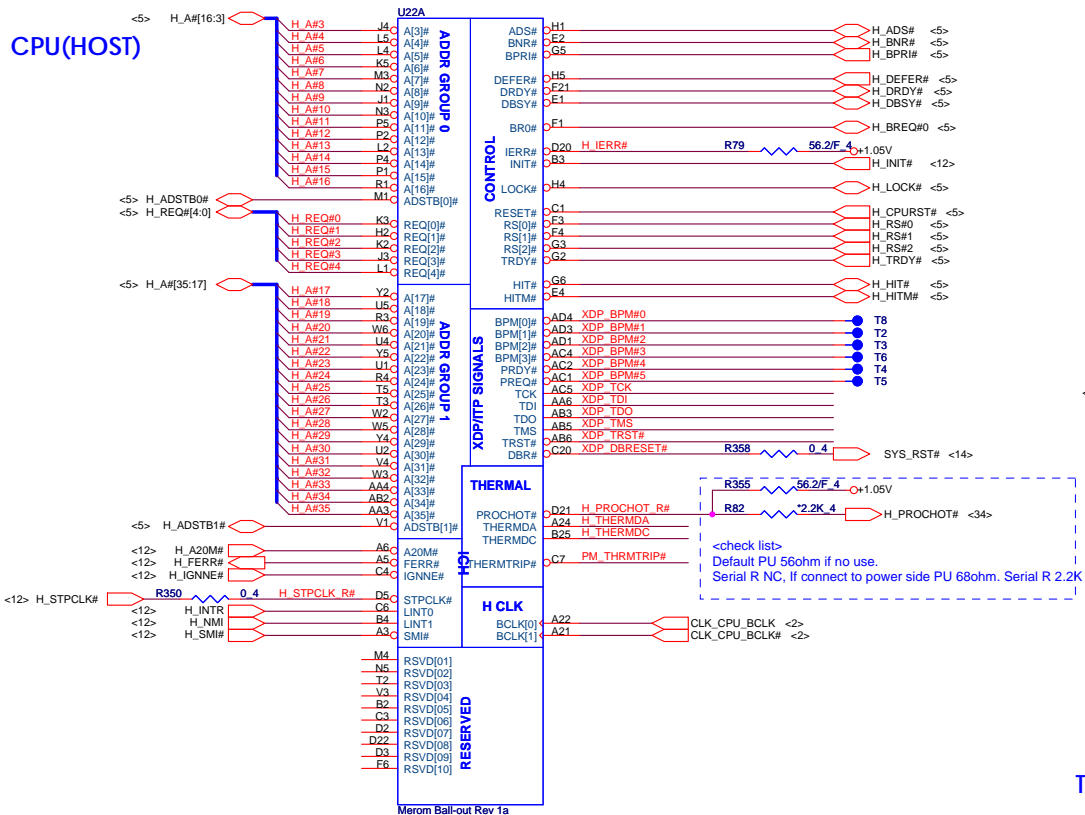


PROJECT : ZD1
Quanta Computer Inc.

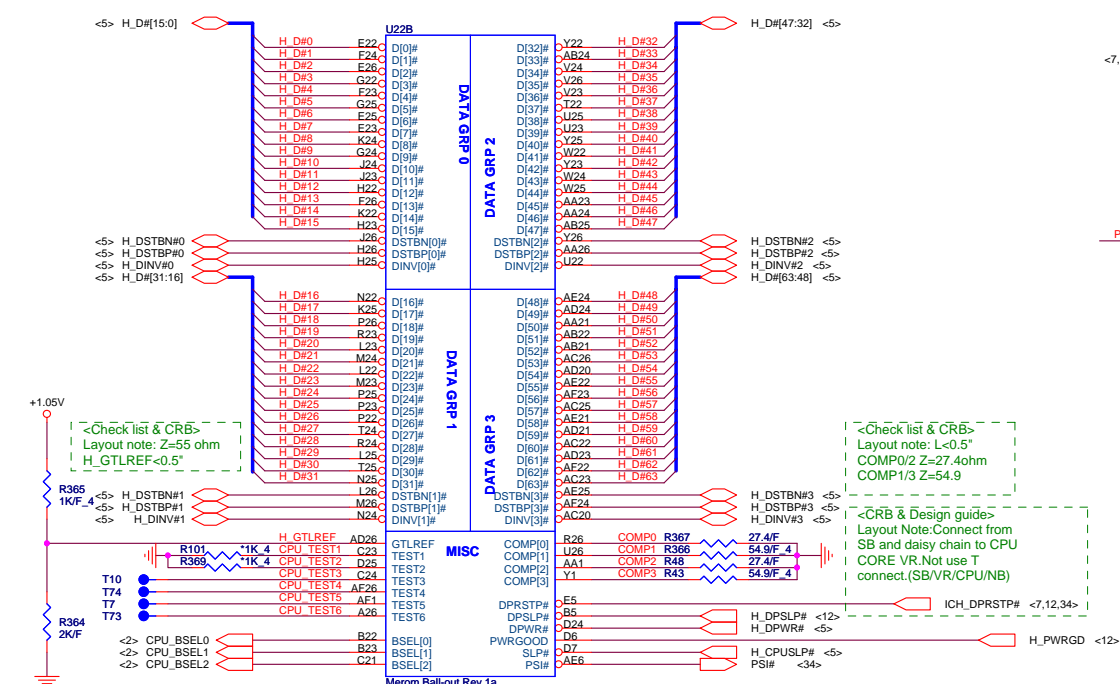
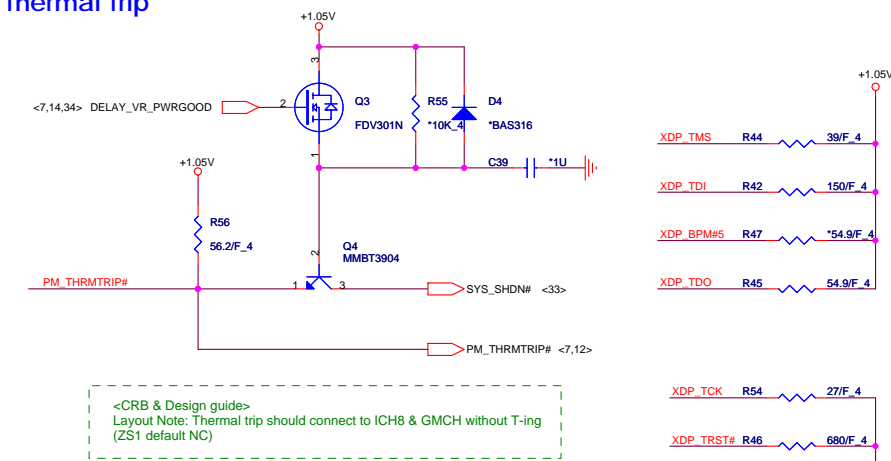
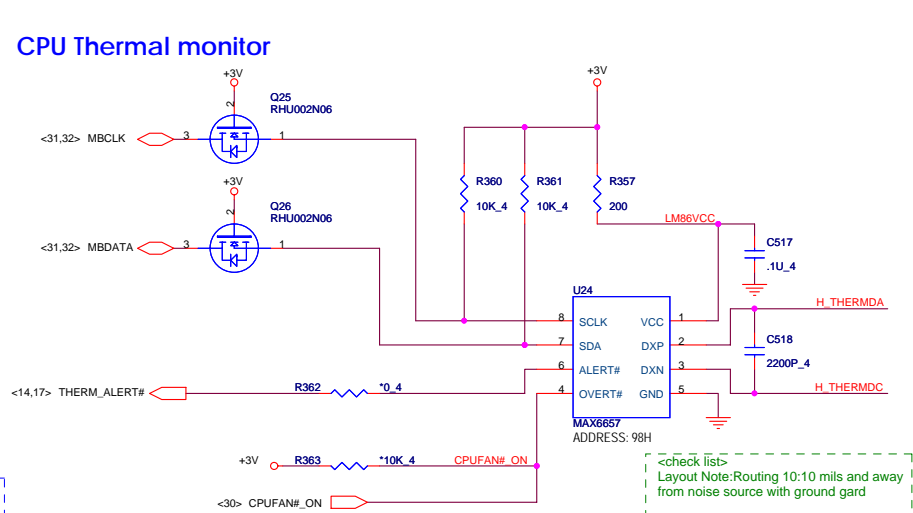
Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	B
Date:	Monday, December 11, 2006	Sheet 2 of 38

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CPU(HOST)

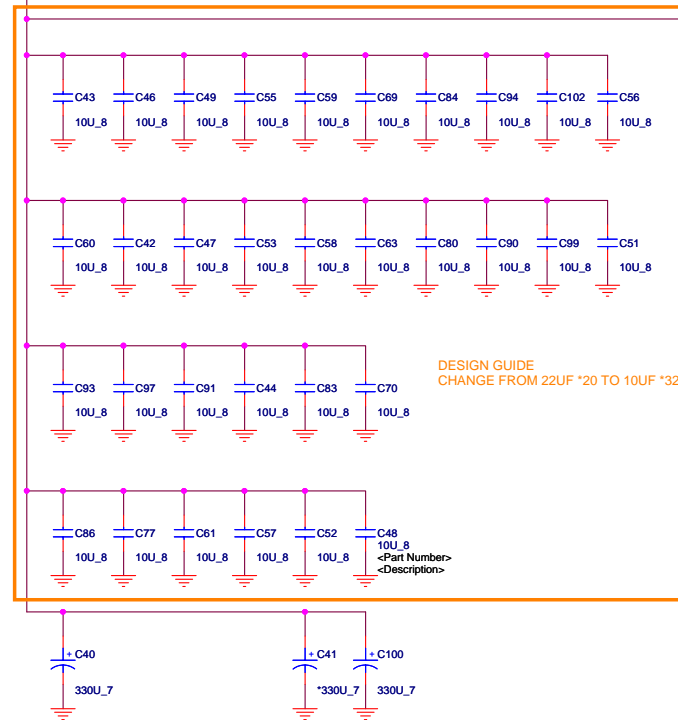


CPU Thermal monitor



CPU(Power)

VCC_CORE

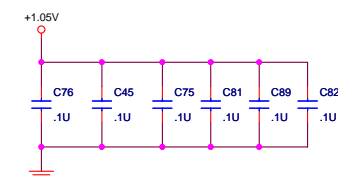


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Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

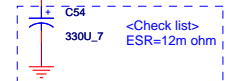
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A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD15
B15	VCC[015]	VCC[082]	AD14
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE3
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	G21 CPU G21
E12	VCC[036]	VCCP[02]	J6 CPU V6
E13	VCC[037]	VCCP[03]	
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	R21
F12	VCC[045]	VCCP[11]	R6
F14	VCC[046]	VCCP[12]	T21
F15	VCC[047]	VCCP[13]	T6
F17	VCC[048]	VCCP[14]	V21
F18	VCC[049]	VCCP[15]	W21
F20	VCC[050]	VCCP[16]	
AA7	VCC[051]		
AA9	VCC[052]	VCCA[01]	B26 +VCCA_PROC
AA10	VCC[053]	VCCA[02]	C26
AA12	VCC[054]		
AA13	VCC[055]		
AA15	VCC[056]	VID[0]	AD6 H_VID0 <34>
AA17	VCC[057]	VID[1]	AE5 H_VID1 <34>
AA18	VCC[058]	VID[2]	AE4 H_VID2 <34>
AA20	VCC[059]	VID[3]	AE3 H_VID3 <34>
AB9	VCC[060]	VID[4]	AE2 H_VID4 <34>
AB10	VCC[061]	VID[5]	AE3 H_VID5 <34>
AB12	VCC[062]	VID[6]	AE2 H_VID6 <34>
AB14	VCC[063]		
AB15	VCC[064]	VCCSENSE	AE7 <34>
AB17	VCC[065]		
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AB18	VCC[067]		

Merom Ball-out Rev 1a

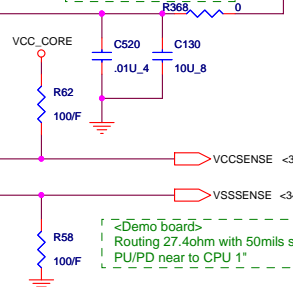
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Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA



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R for test only
R75 CPU G21
R63 CPU V6
0.4
0.4

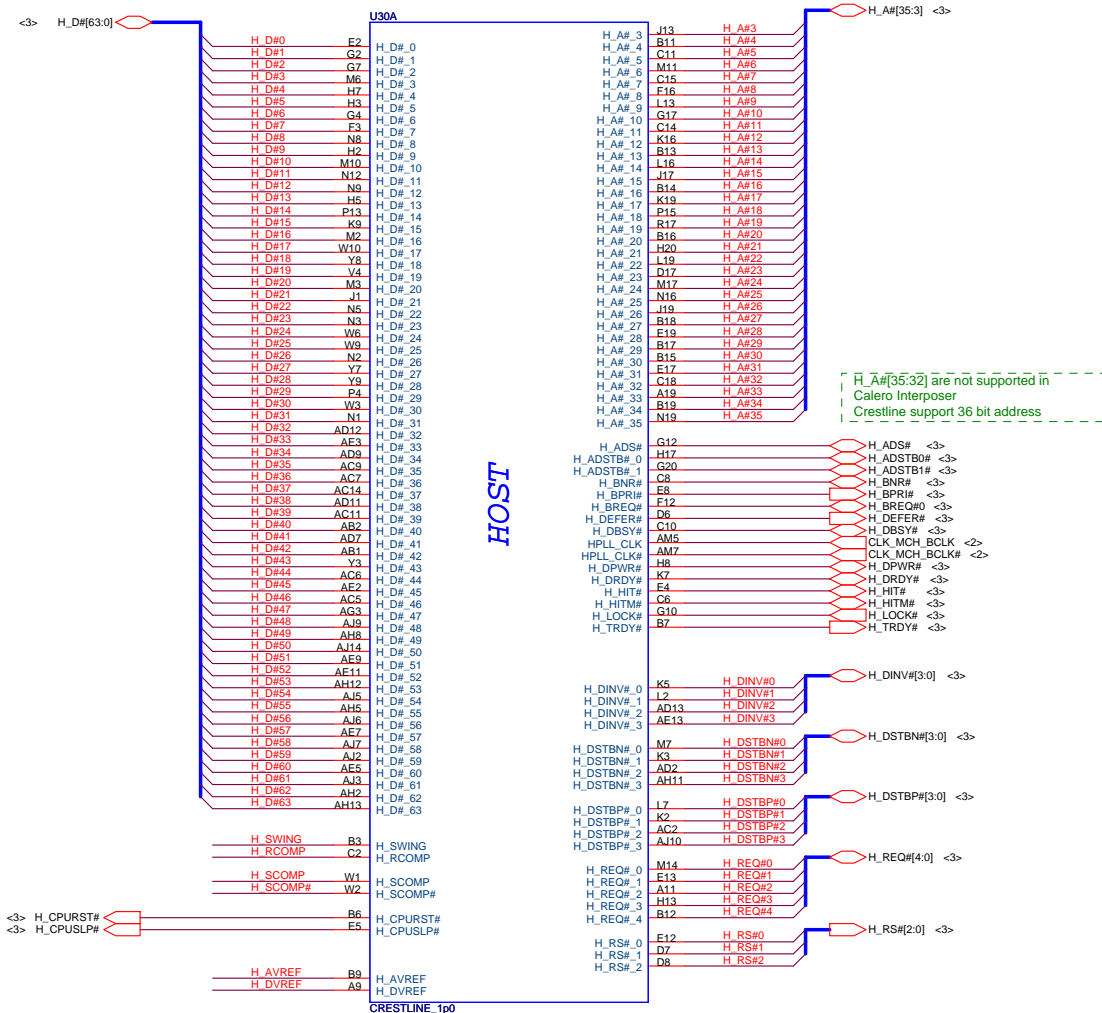
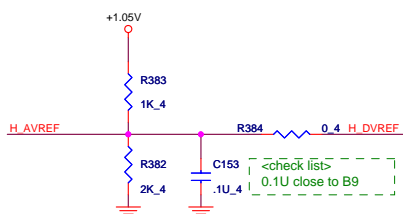
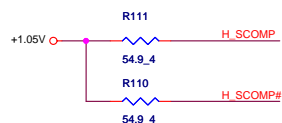
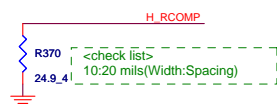
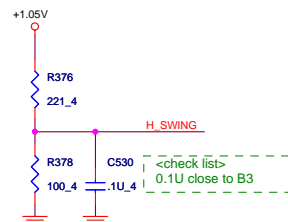


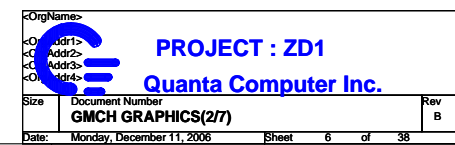
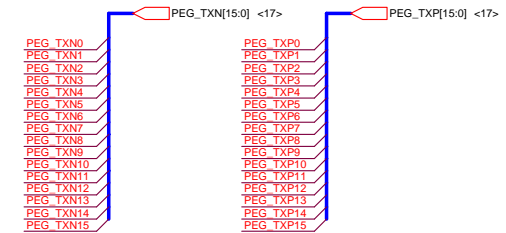
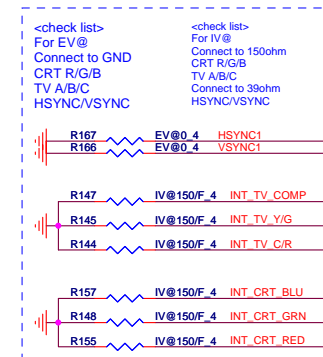
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.01U near to B26 ball
R368
0



U22D			
A4	VSS[001]	VSS[082]	P21
A8	VSS[002]	VSS[083]	P24
A11	VSS[003]	VSS[084]	R2
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
AF2	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U24
B19	VSS[014]	VSS[095]	V2
B21	VSS[015]	VSS[096]	V5
B24	VSS[016]	VSS[097]	V25
C5	VSS[017]	VSS[098]	W1
C8	VSS[018]	VSS[099]	W2
C11	VSS[019]	VSS[100]	W4
C14	VSS[020]	VSS[101]	W23
C16	VSS[021]	VSS[102]	Y3
C19	VSS[022]	VSS[103]	Y6
C2	VSS[023]	VSS[104]	Y24
C22	VSS[024]	VSS[105]	AA2
C25	VSS[025]	VSS[106]	AA5
D1	VSS[026]	VSS[107]	AA8
D4	VSS[027]	VSS[108]	AA14
D8	VSS[028]	VSS[109]	AA16
D11	VSS[029]	VSS[110]	AA22
D13	VSS[030]	VSS[111]	AA25
D16	VSS[031]	VSS[112]	AB1
D19	VSS[032]	VSS[113]	AB4
D23	VSS[033]	VSS[114]	AB11
D26	VSS[034]	VSS[115]	AB16
E3	VSS[035]	VSS[116]	AB19
E6	VSS[036]	VSS[117]	AB23
E8	VSS[037]	VSS[118]	AC3
E11	VSS[038]	VSS[119]	AC6
E14	VSS[039]	VSS[120]	AC8
E16	VSS[040]	VSS[121]	AC11
E19	VSS[041]	VSS[122]	AC14
E21	VSS[042]	VSS[123]	AC16
E24	VSS[043]	VSS[124]	AC21
F5	VSS[044]	VSS[125]	AC24
F8	VSS[045]	VSS[126]	AD2
F11	VSS[046]	VSS[127]	AD5
F13	VSS[047]	VSS[128]	AD8
F16	VSS[048]	VSS[129]	AD11
F19	VSS[049]	VSS[130]	AD13
F2	VSS[050]	VSS[131]	AD16
F22	VSS[051]	VSS[132]	AD19
F24	VSS[052]	VSS[133]	AD22
G4	VSS[053]	VSS[134]	AD25
G1	VSS[054]	VSS[135]	AE1
G23	VSS[055]	VSS[136]	AE4
G26	VSS[056]	VSS[137]	AE8
H3	VSS[057]	VSS[138]	AE11
H6	VSS[058]	VSS[139]	AE14
H21	VSS[059]	VSS[140]	AE16
H24	VSS[060]	VSS[141]	AE19
J2	VSS[061]	VSS[142]	AE23
J22	VSS[062]	VSS[143]	AE26
J26	VSS[063]	VSS[144]	AF6
K1	VSS[064]	VSS[145]	AF8
K4	VSS[065]	VSS[146]	AF11
K23	VSS[066]	VSS[147]	AF13
K26	VSS[067]	VSS[148]	AF16
L3	VSS[068]	VSS[149]	AF19
L6	VSS[069]	VSS[150]	AF21
L21	VSS[070]	VSS[151]	A25
L24	VSS[071]	VSS[152]	AF25
M2	VSS[072]	VSS[153]	
M2	VSS[073]	VSS[154]	
M5	VSS[074]	VSS[155]	
M22	VSS[075]	VSS[156]	
M25	VSS[076]	VSS[157]	
N1	VSS[077]	VSS[158]	
N4	VSS[078]	VSS[159]	
N23	VSS[079]	VSS[160]	
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		VSS[163]	

Merom Ball-out Rev 1a



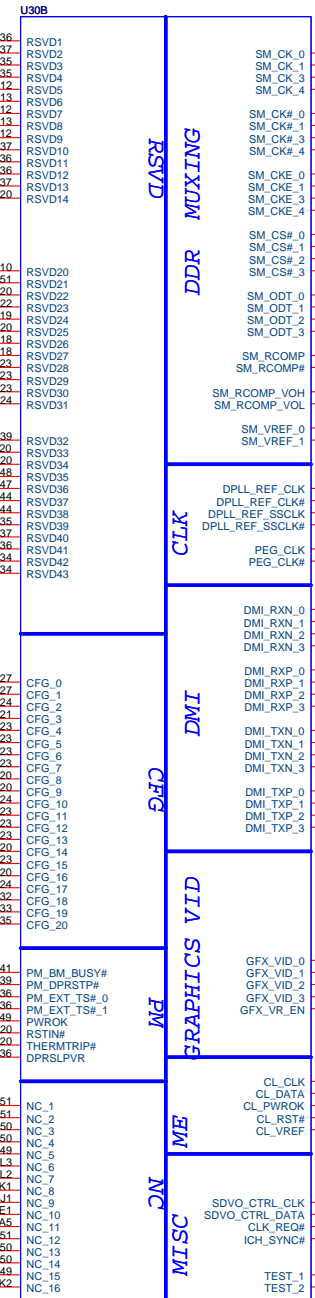
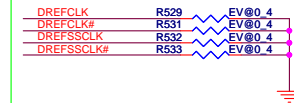
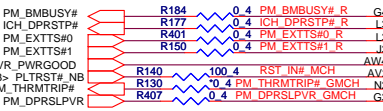
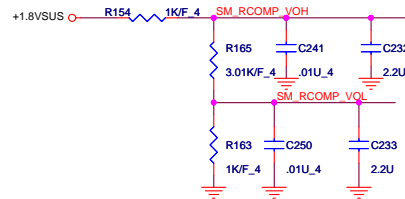
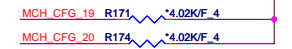
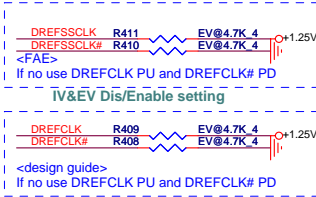
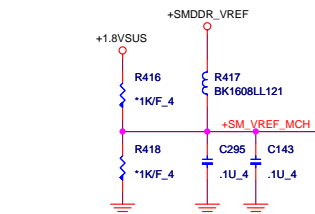
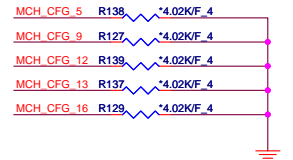
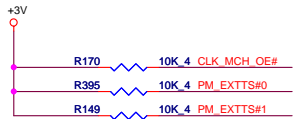
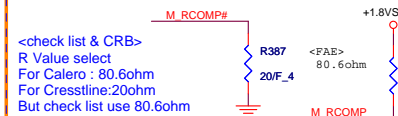


Strapping table

All strap are sampled with respect to the leading edge of the GMCH power ok signal
CFG[17:3] have internal pull-up
CFG[18:19] have internal pull-down
Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reserved Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation 1 = Reverse Lanes (Default)
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

INTEL CRB
CRESTLINE SHOULD USE 200OHM

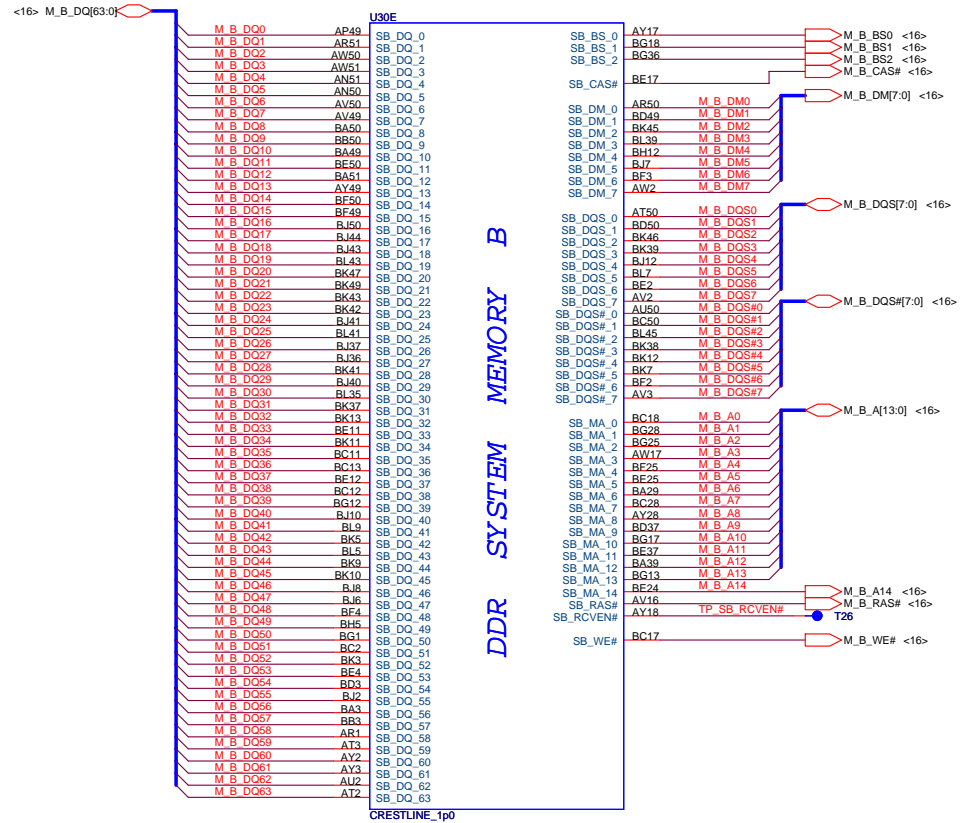
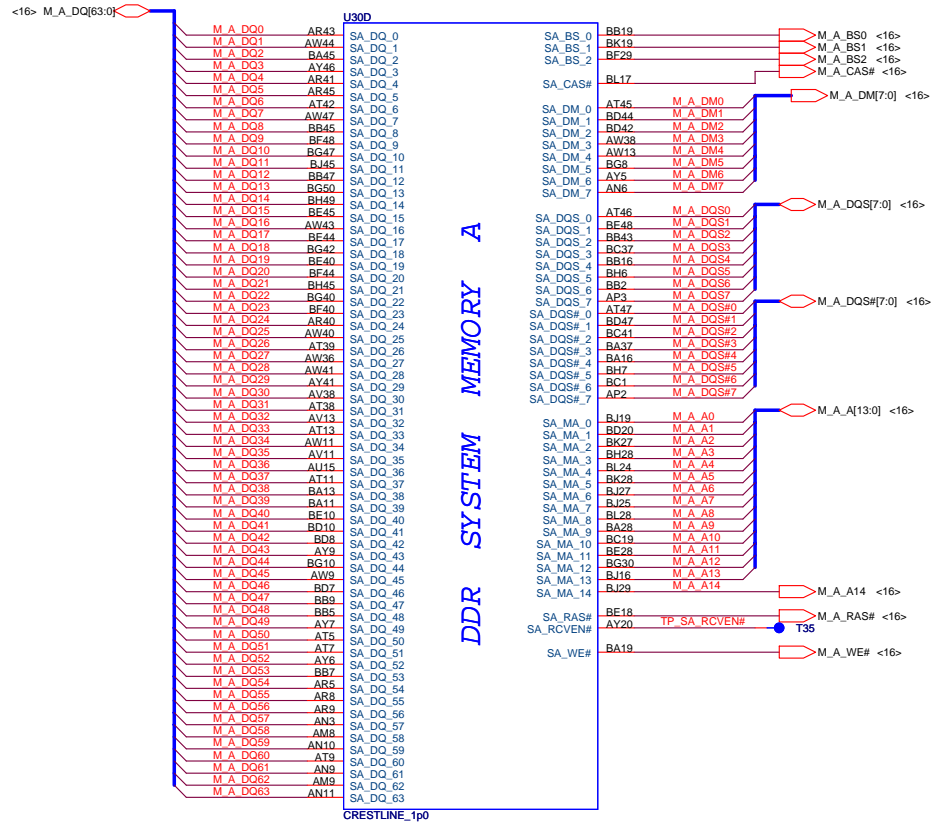


CRESTLINE_1p0

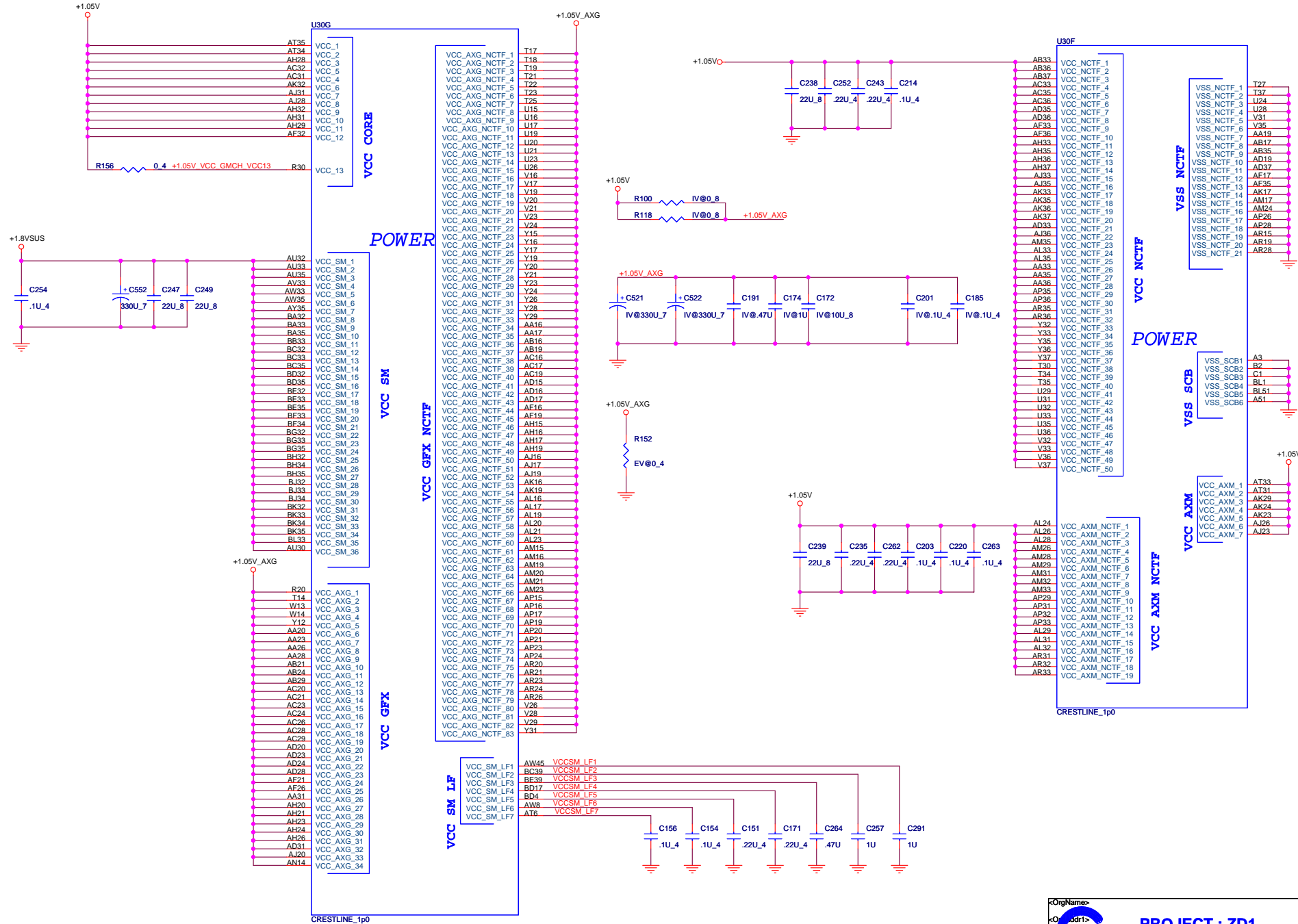
INTEL FAE suggest PD for external graphics

PROJECT : ZD1
Quanta Computer Inc.

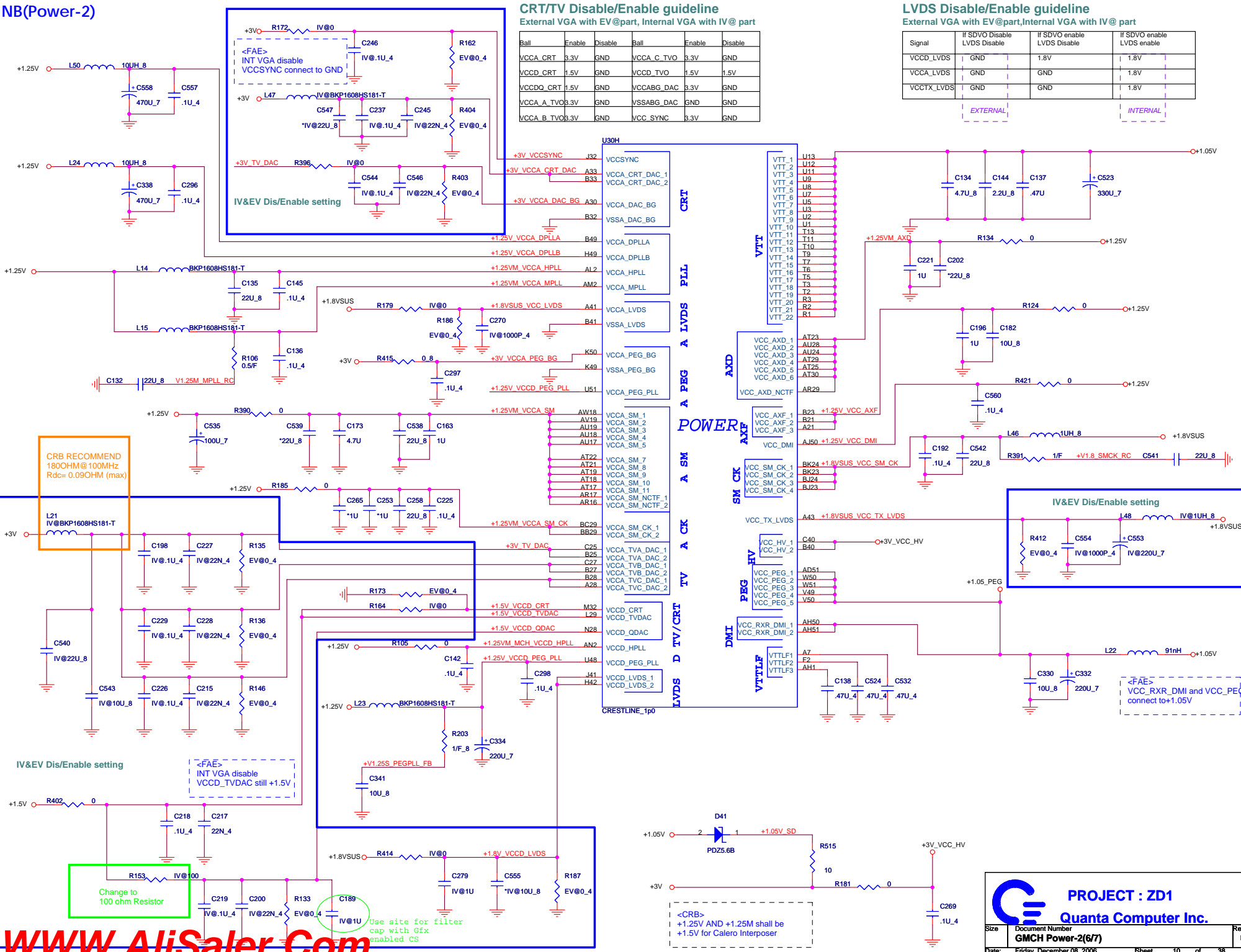
Size	Document Number	Rev
	GMCH (STRAPPING/OTHER 3/7)	B
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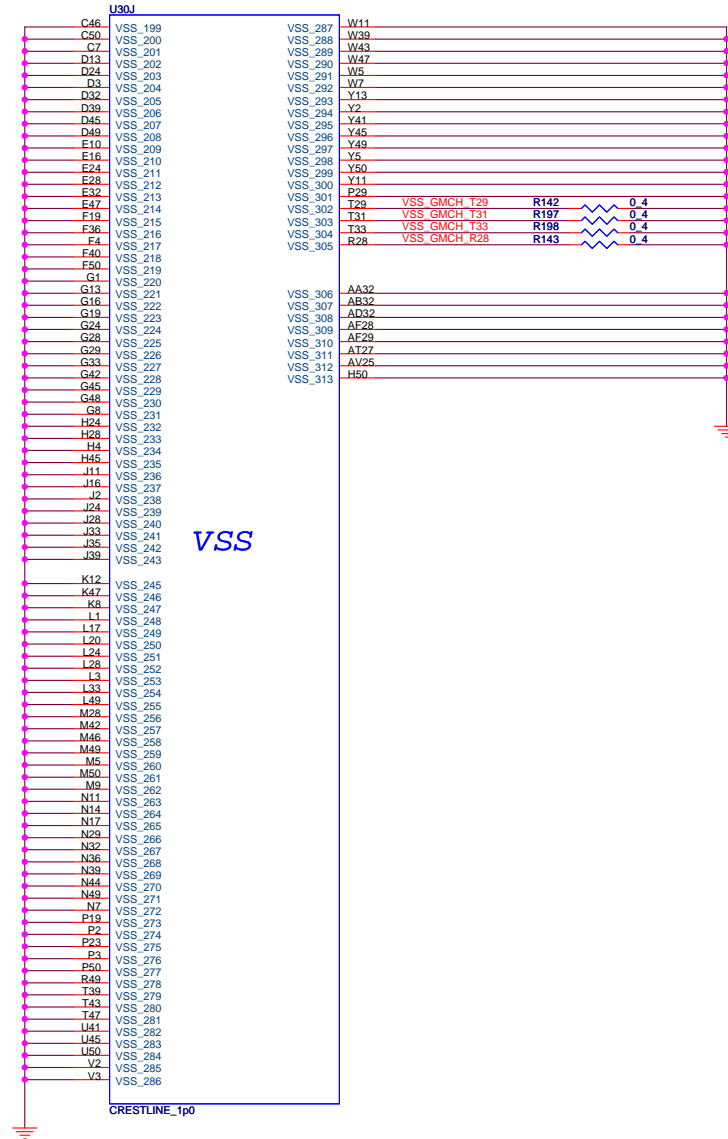
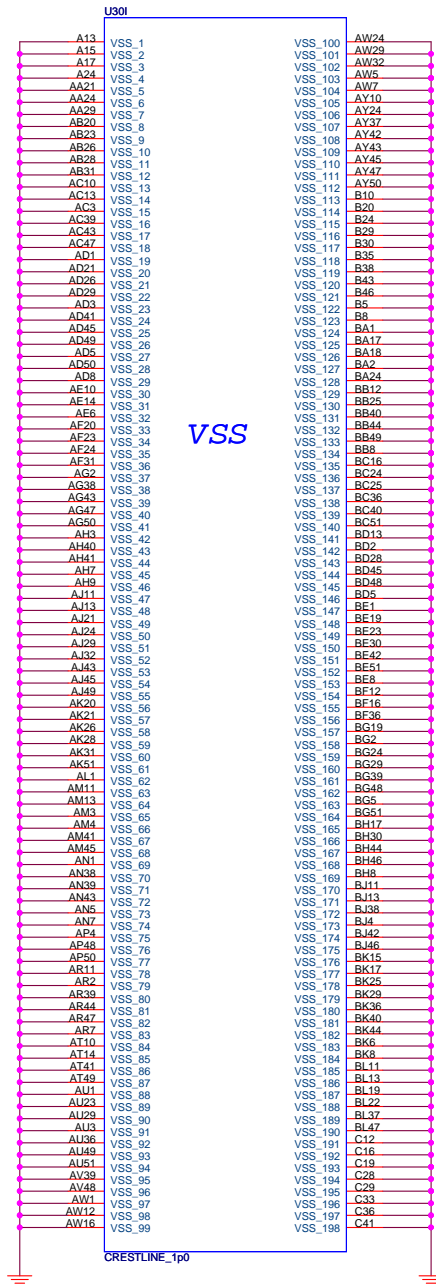


NB(Power-1)

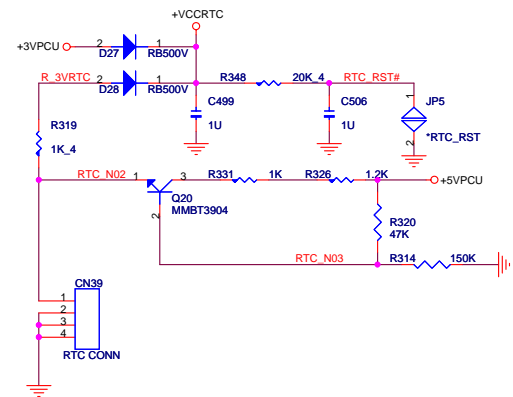


NB(Power-2)

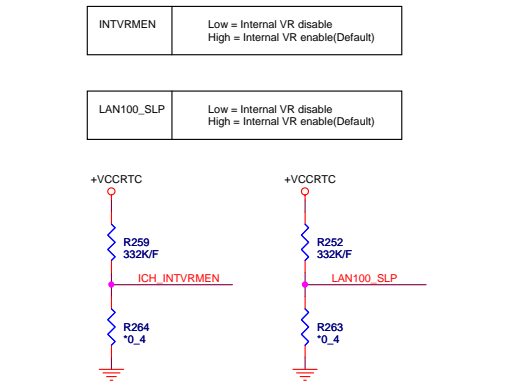




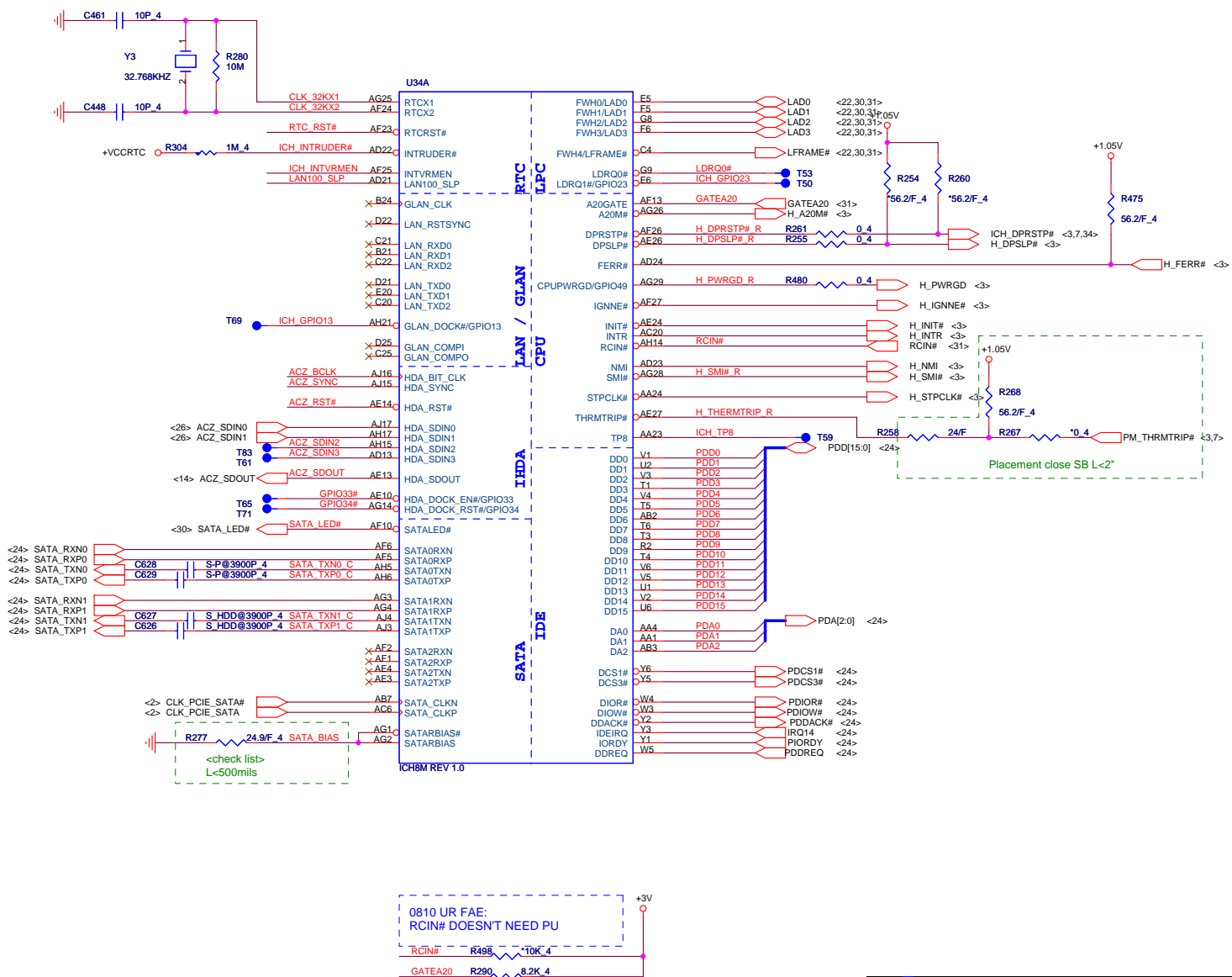
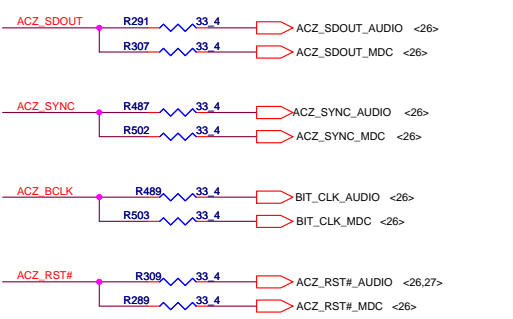
RTC



SB Strap

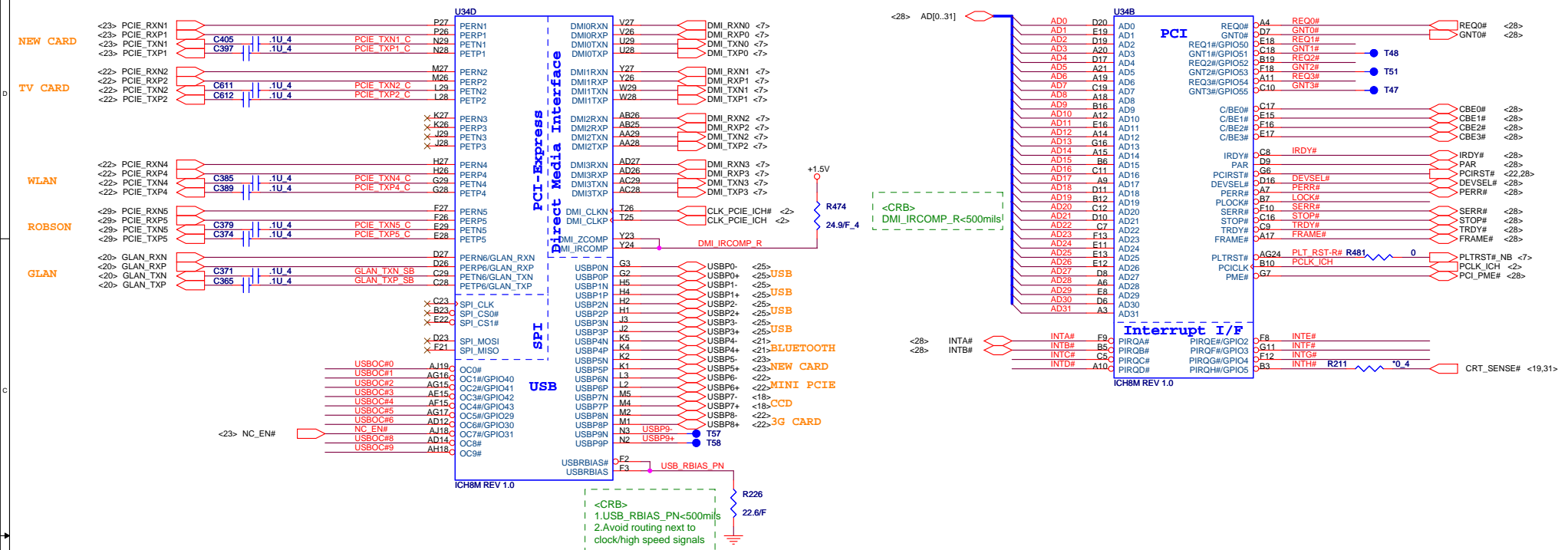


HDA



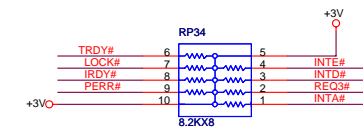
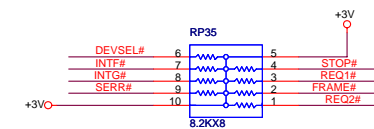
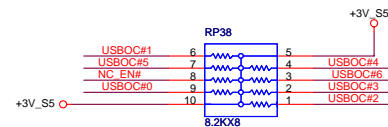
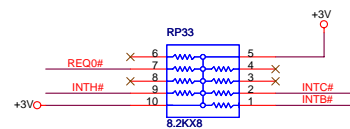
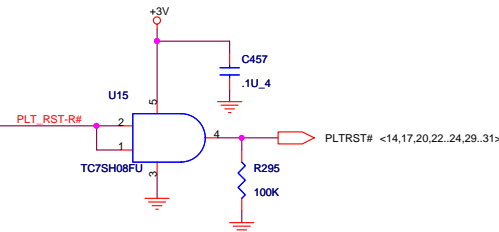
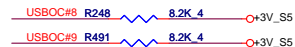
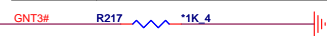
SB-PCIE/USB/DMI

SB-PCI



A16 SWAP Override strap

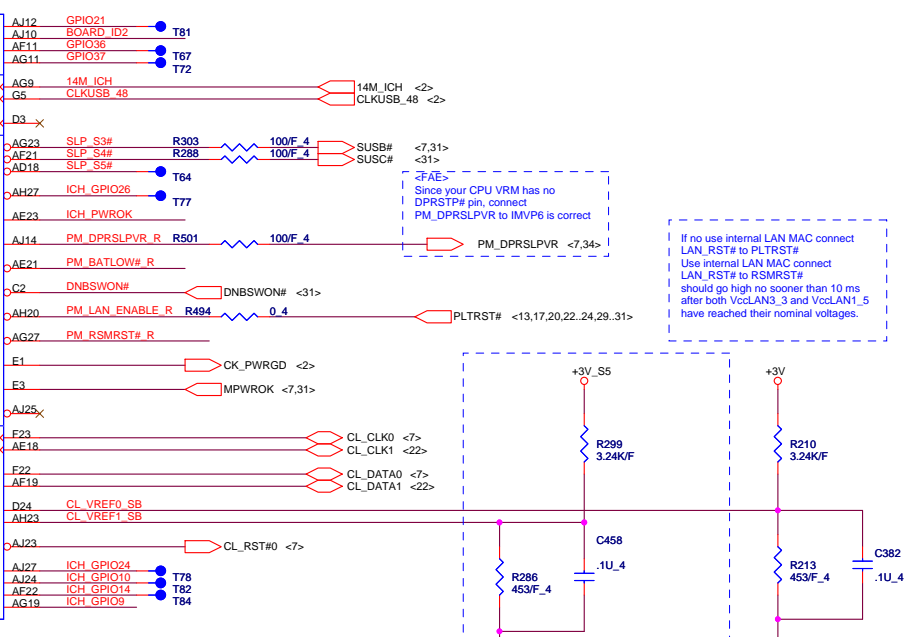
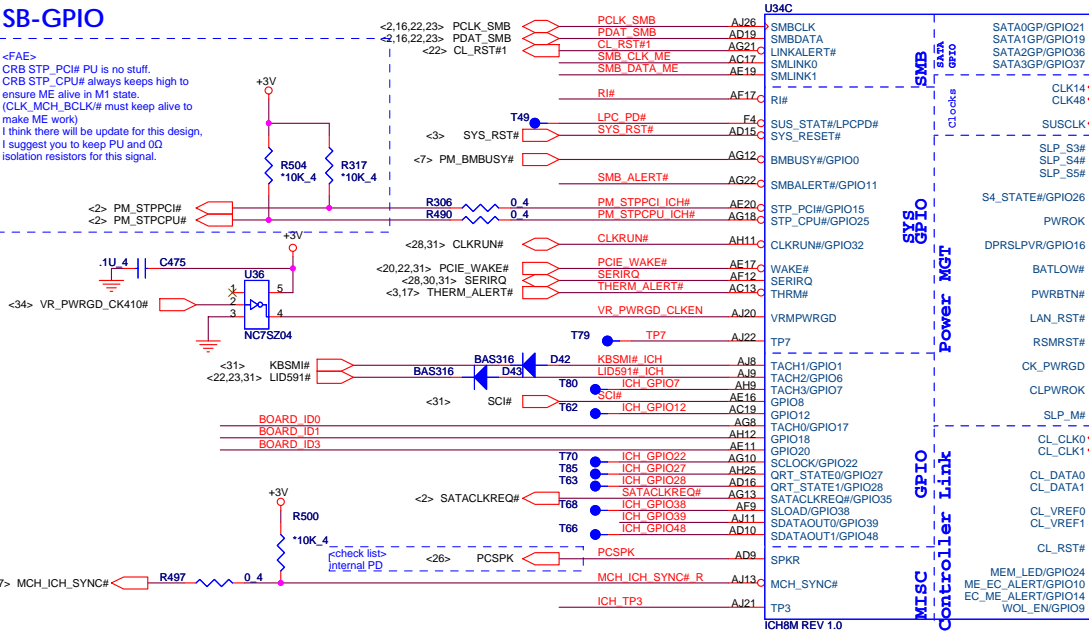
PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---------------------------------------------------



PROJECT : ZD1
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SB-GPIO

<FAE>
CRB STP_CPU# PU is no stuff.
CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
(CLK, MCH, BCLK# must keep alive to make ME work)
I think there will be update for this design.
I suggest you to keep PU and OQ isolation resistors for this signal.

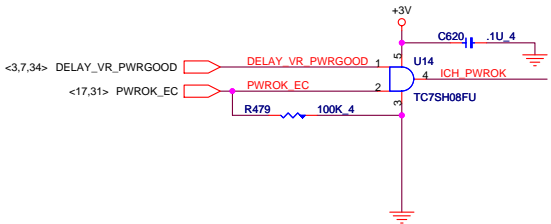
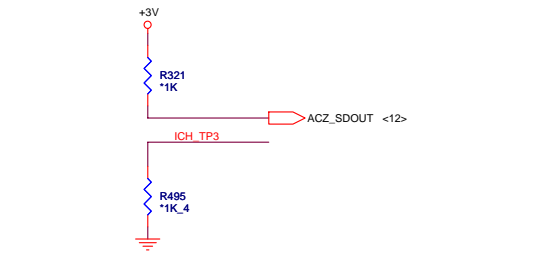
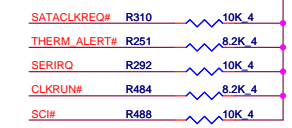
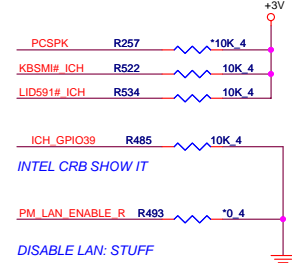
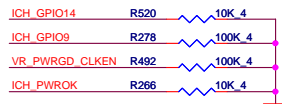
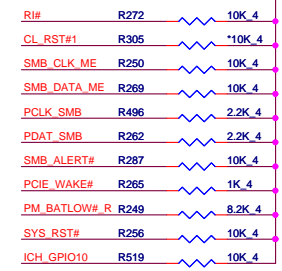
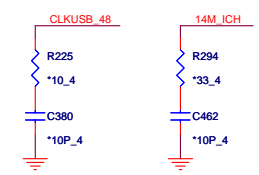


No Reboot strap

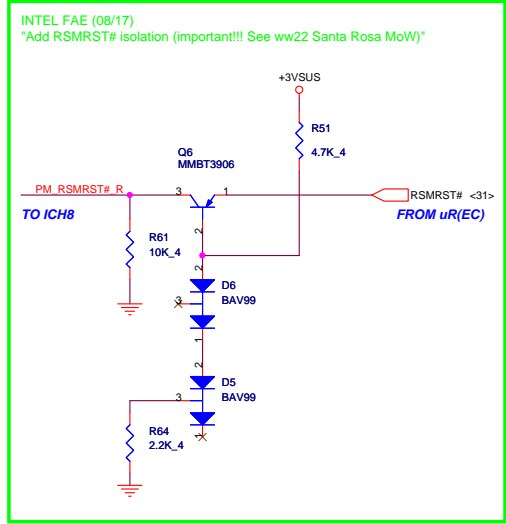
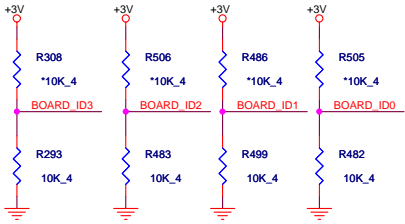
HDA_SPKR	Low = Default High = No Reboot
----------	-----------------------------------

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

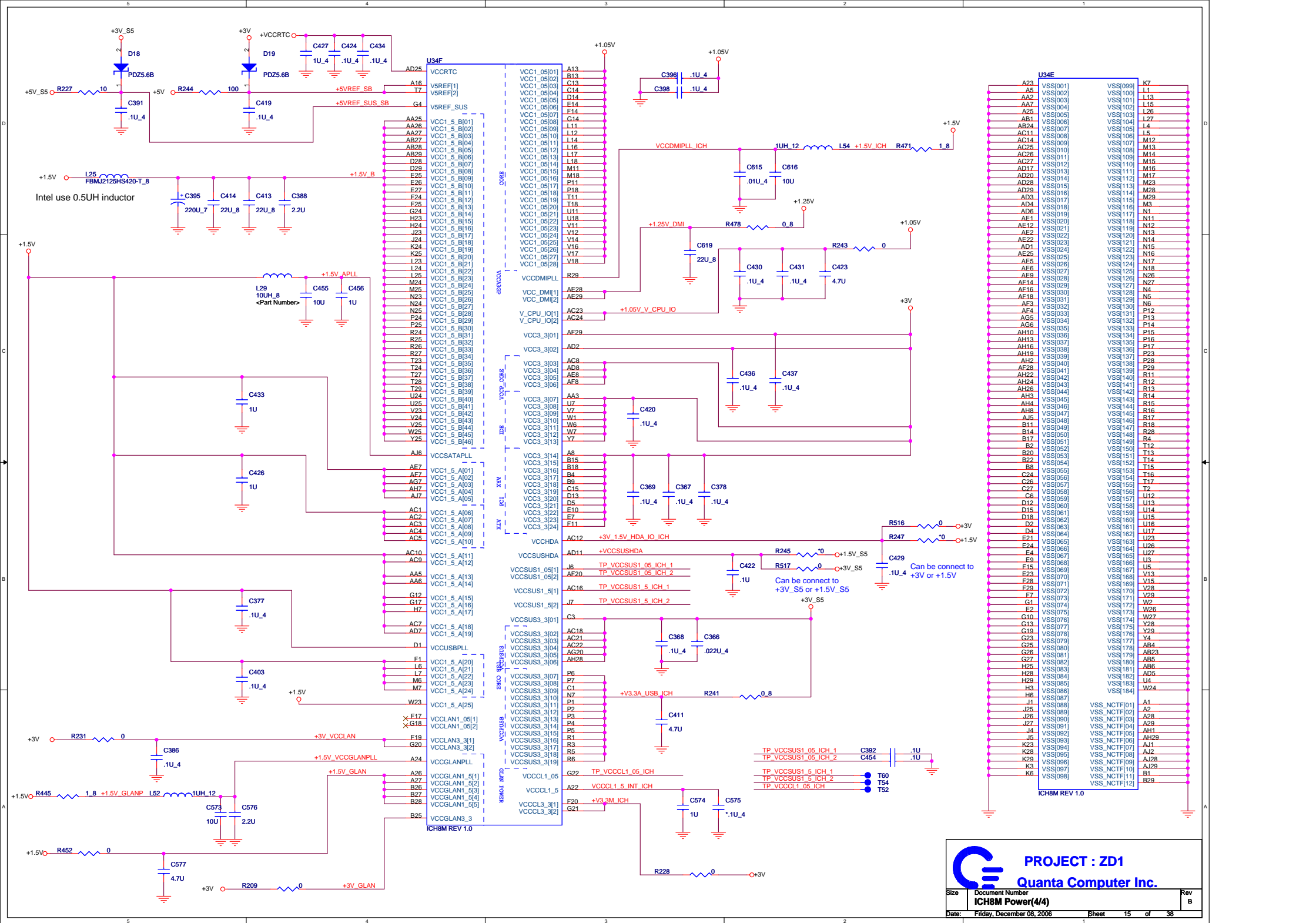


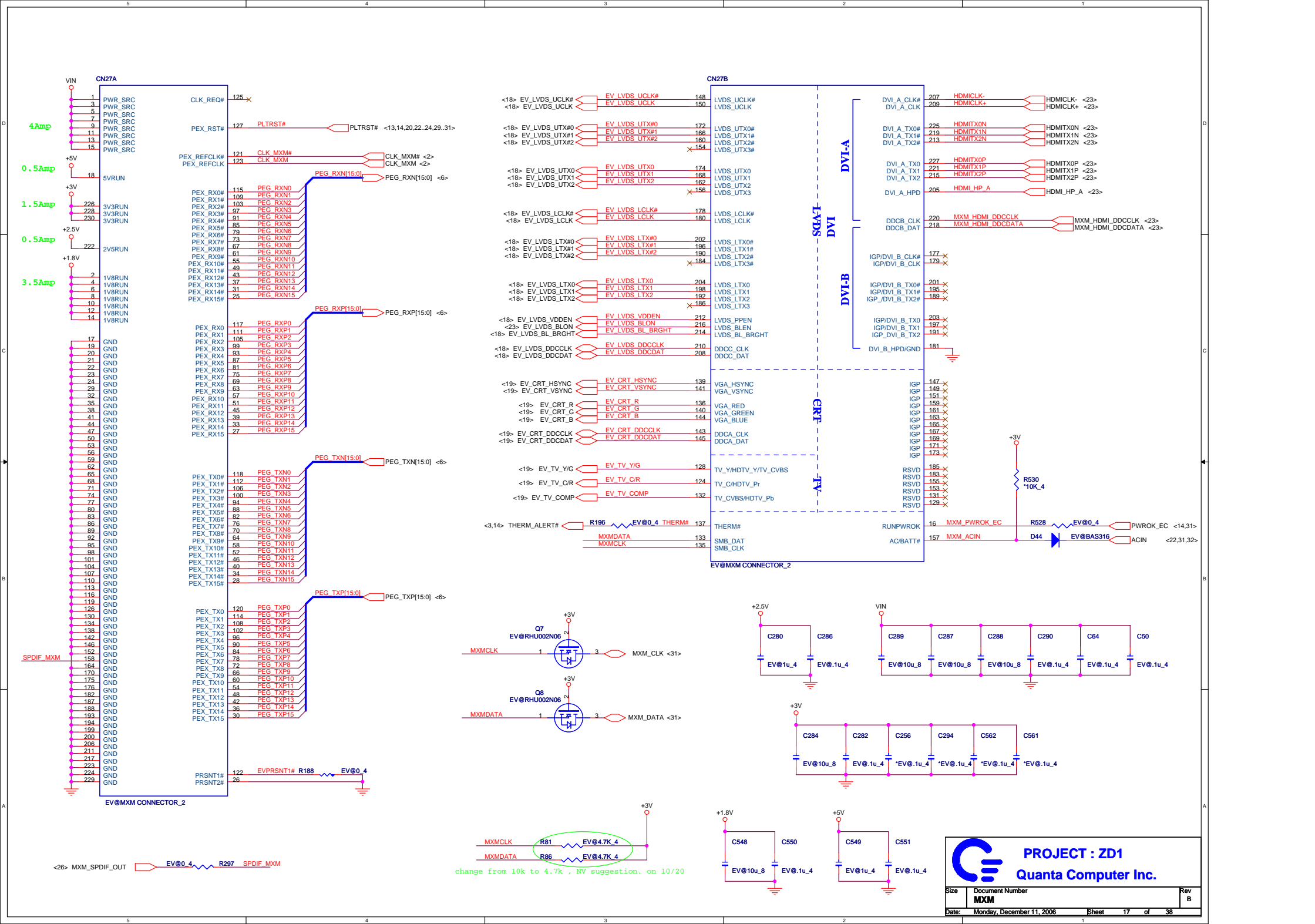
Board ID	ID3	ID2	ID1	ID0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0



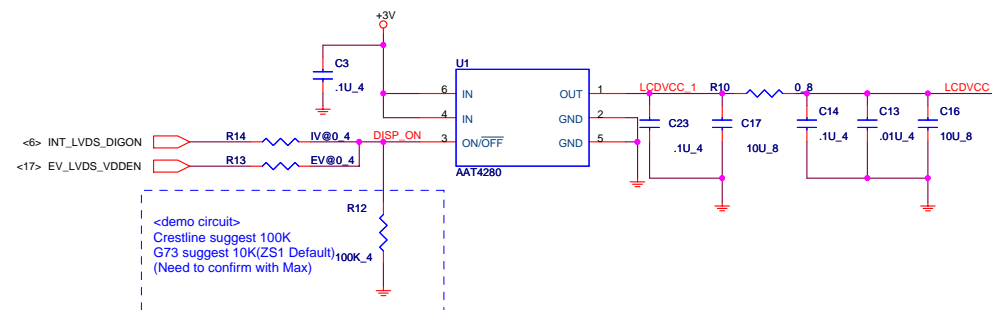
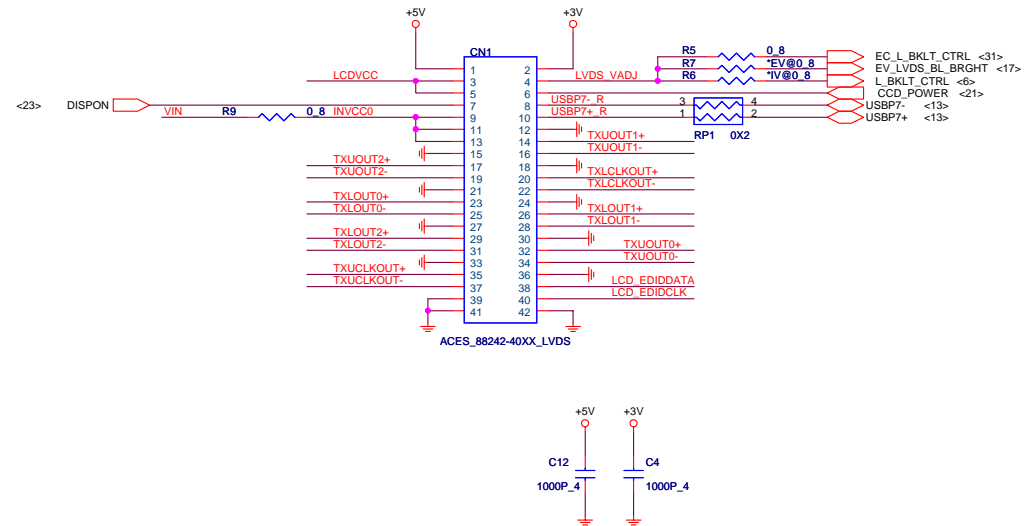
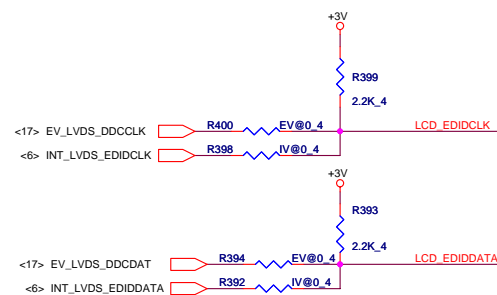
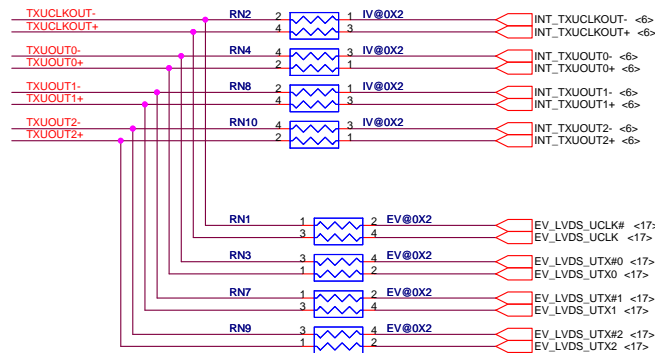
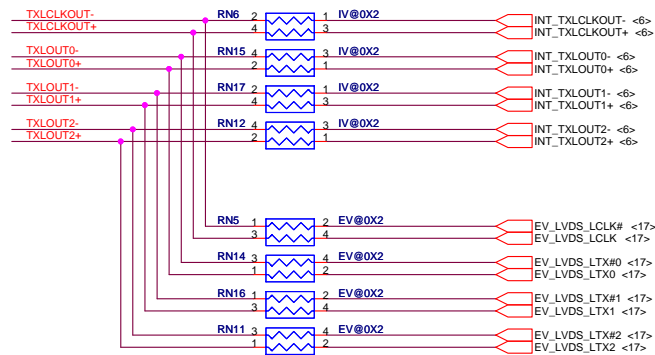
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	ICH8M GPIO(3/4)	B
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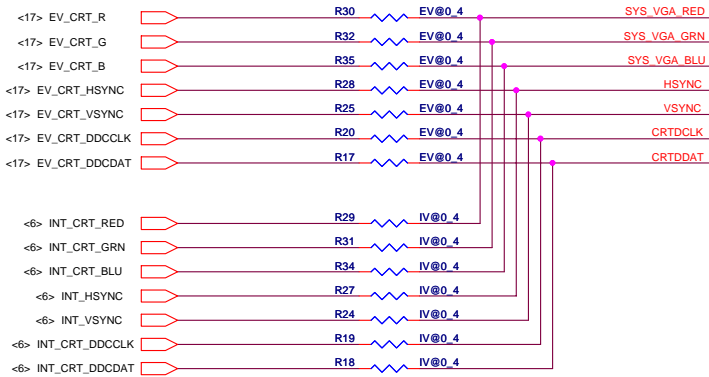




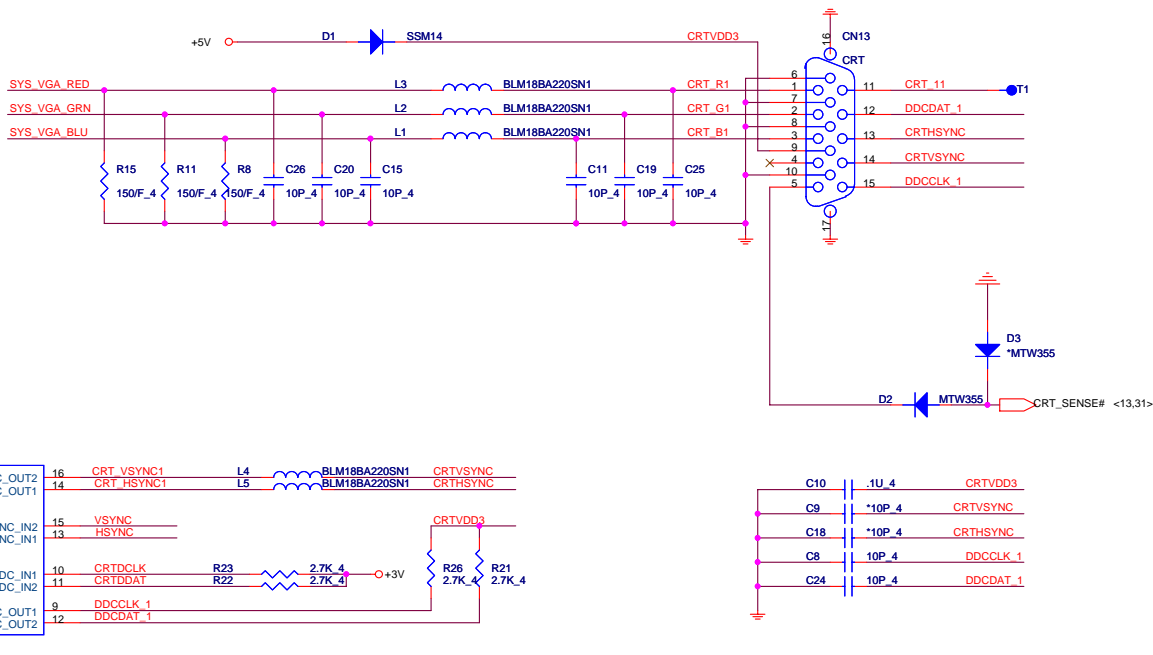
LVDS



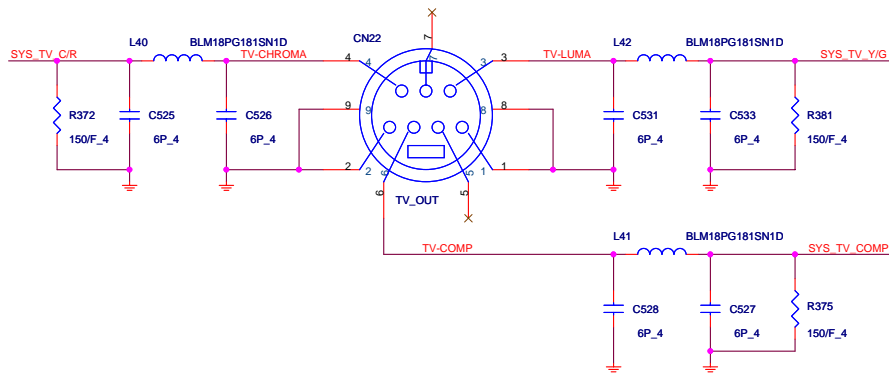
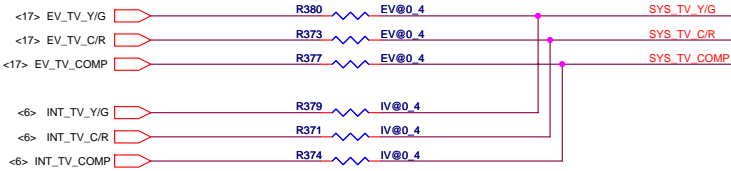
CRT Select



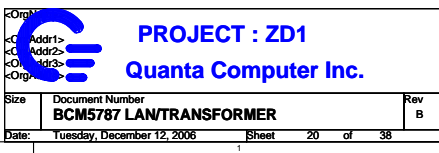
CRT CONNECTOR AND ESD



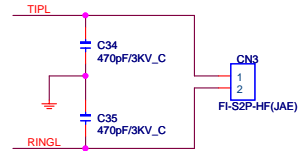
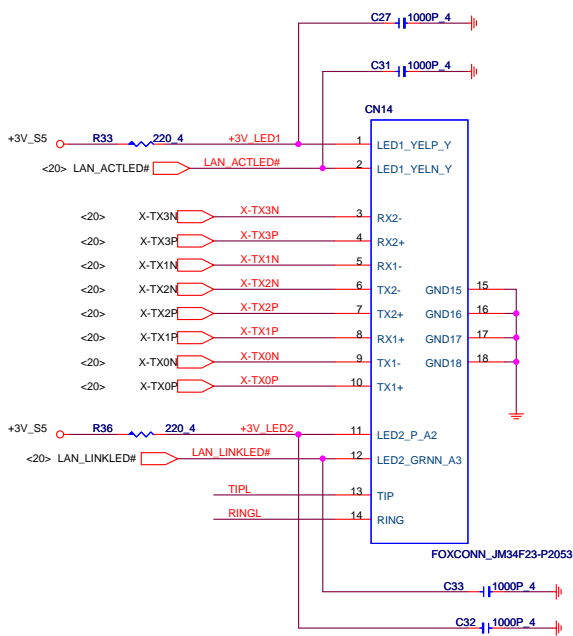
TV Out (SVHS) MiniDIN 7-pin



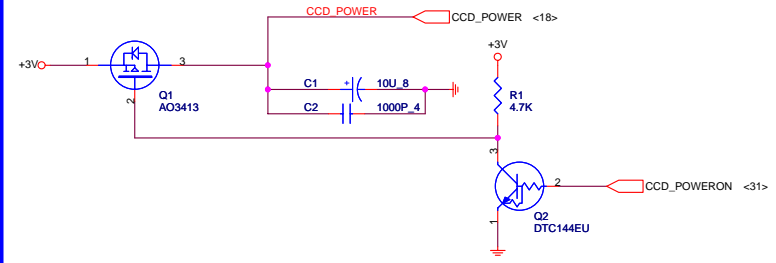
WWW.AliSaler.Com



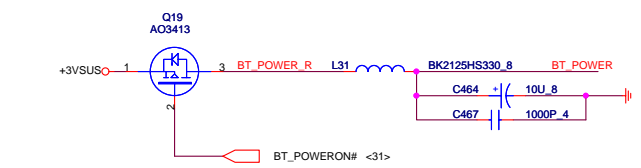
RJ45-11



CAMERA MODULE CONNECTOR

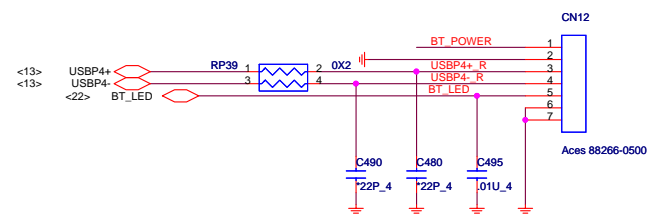
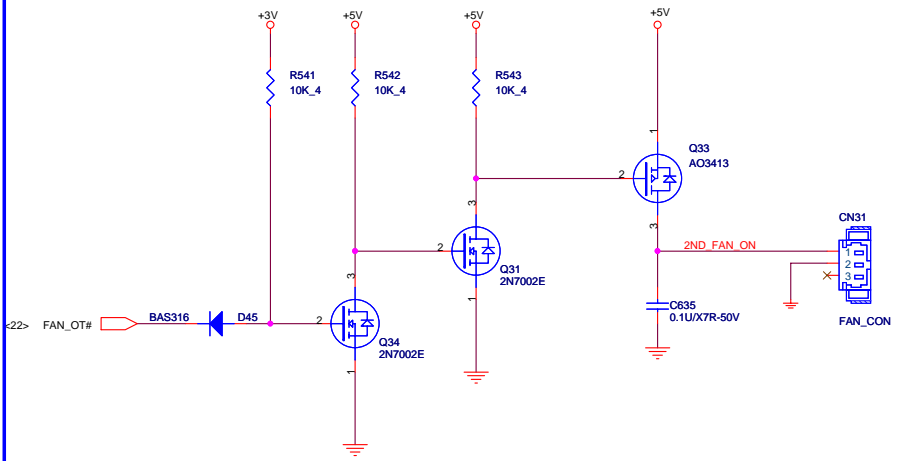
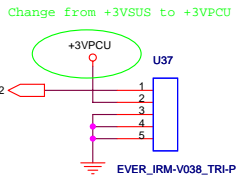


BLUETOOTH MODULE CONNECTOR

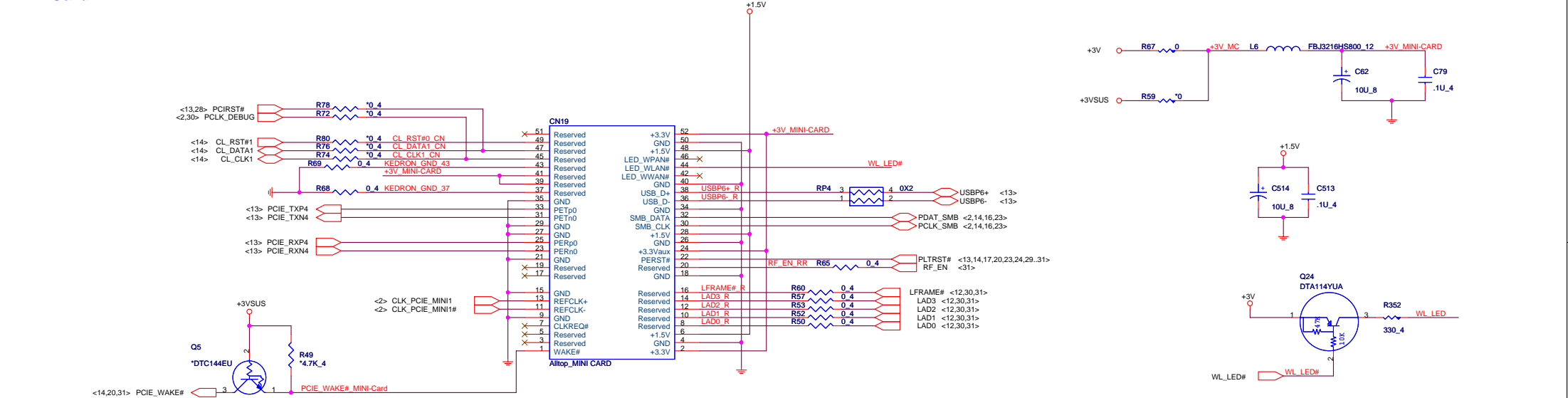


CIR

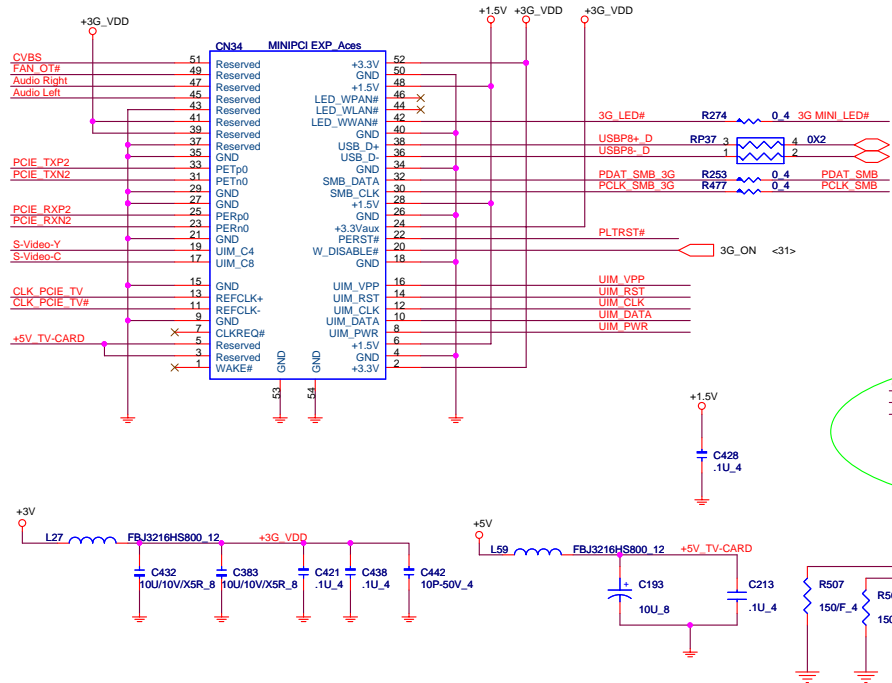
2nd FAN



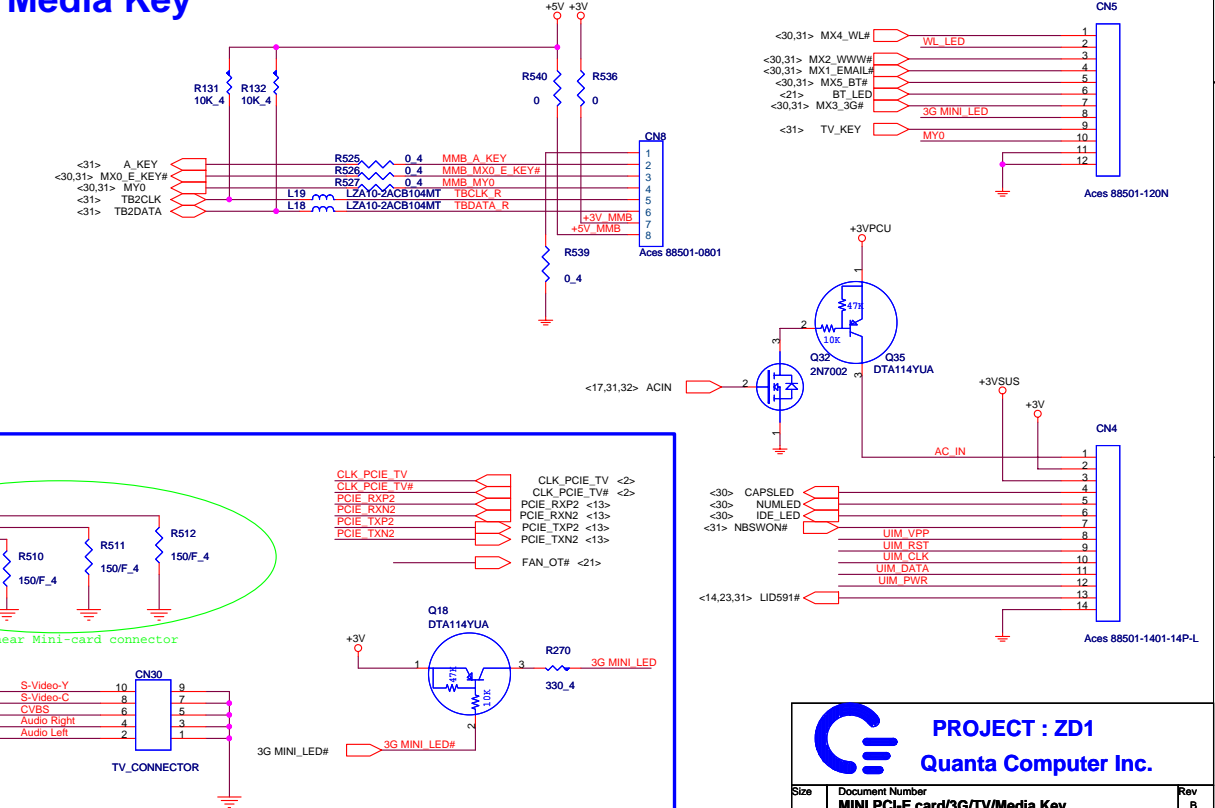
MINI-Card



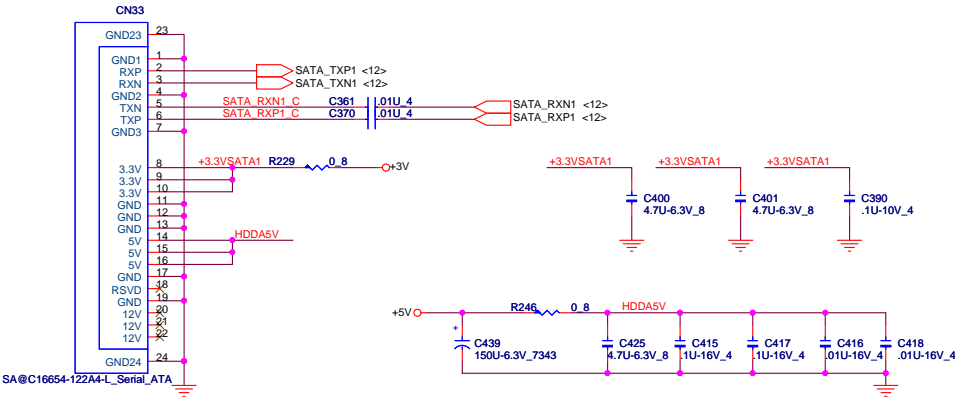
3G/TV MINI CARD



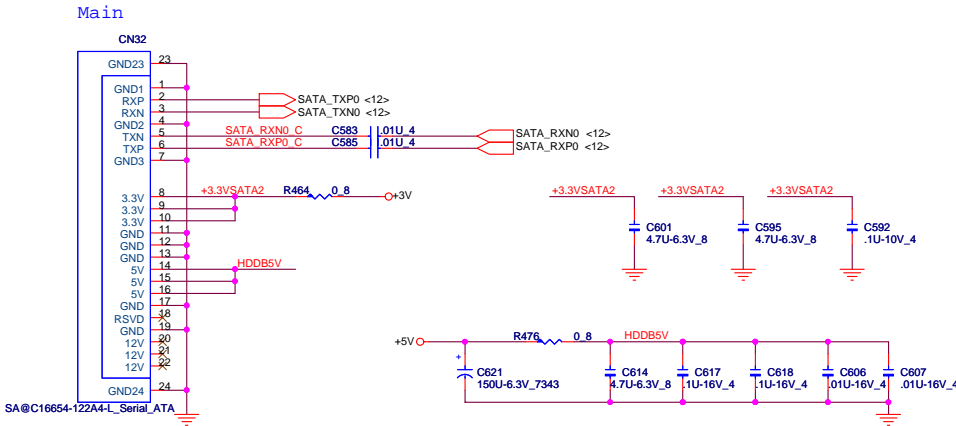
Media Key



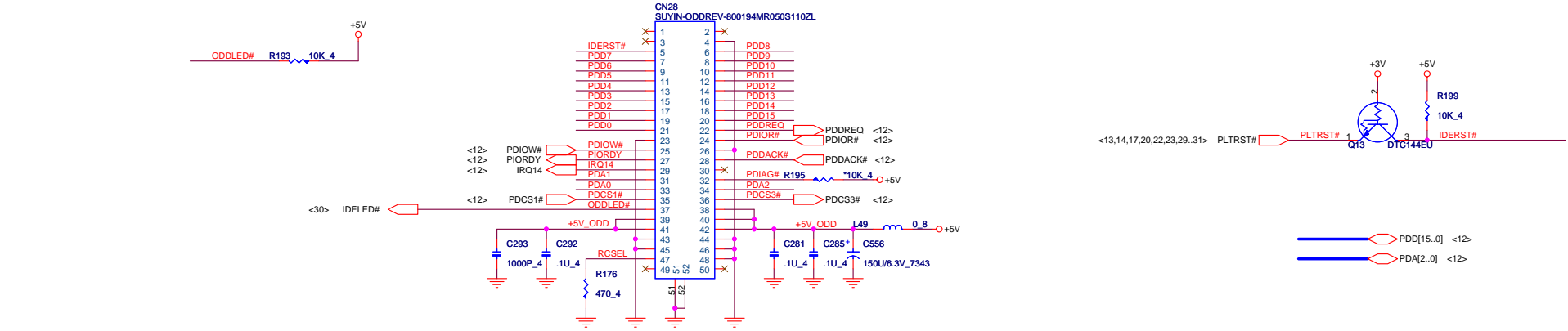
SATA HDD1



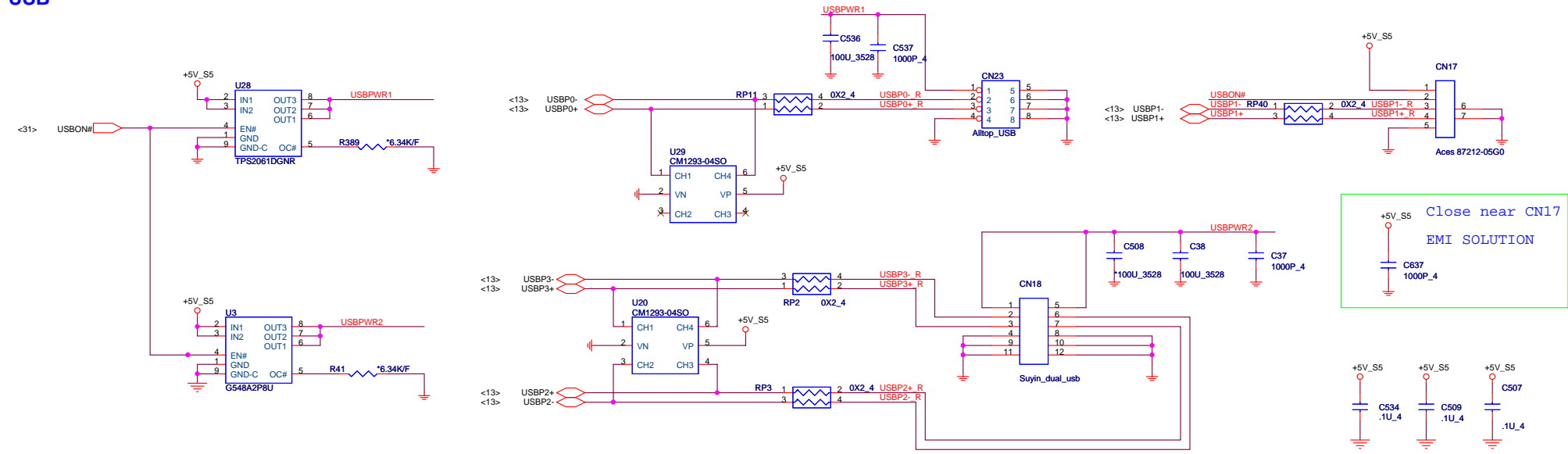
SATA HDD2



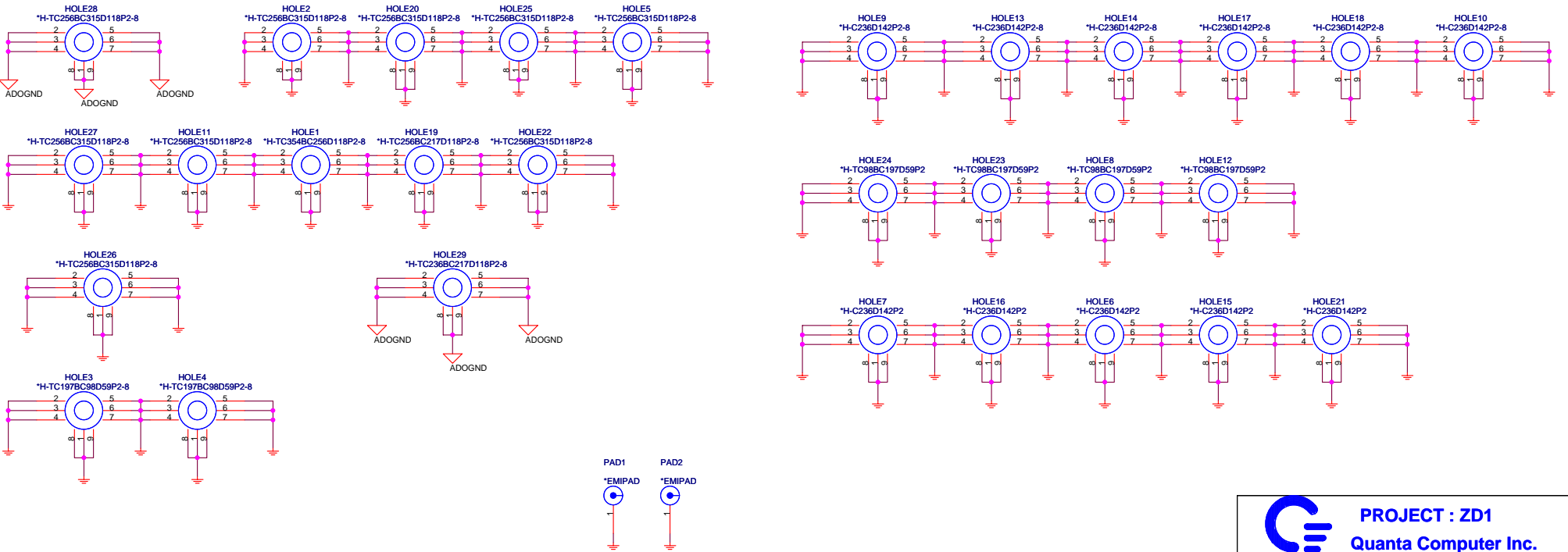
ODD (PATA)



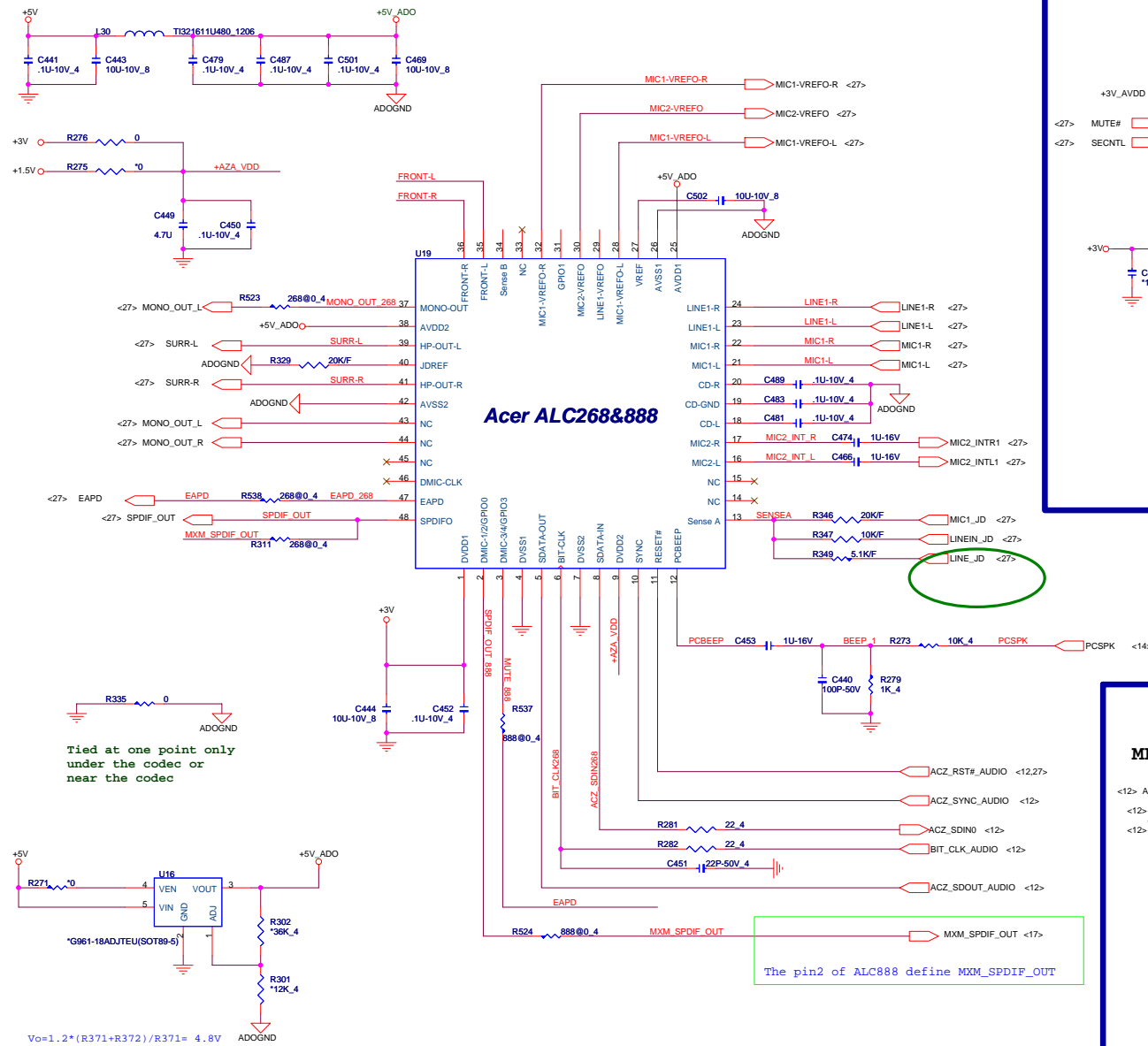
USB



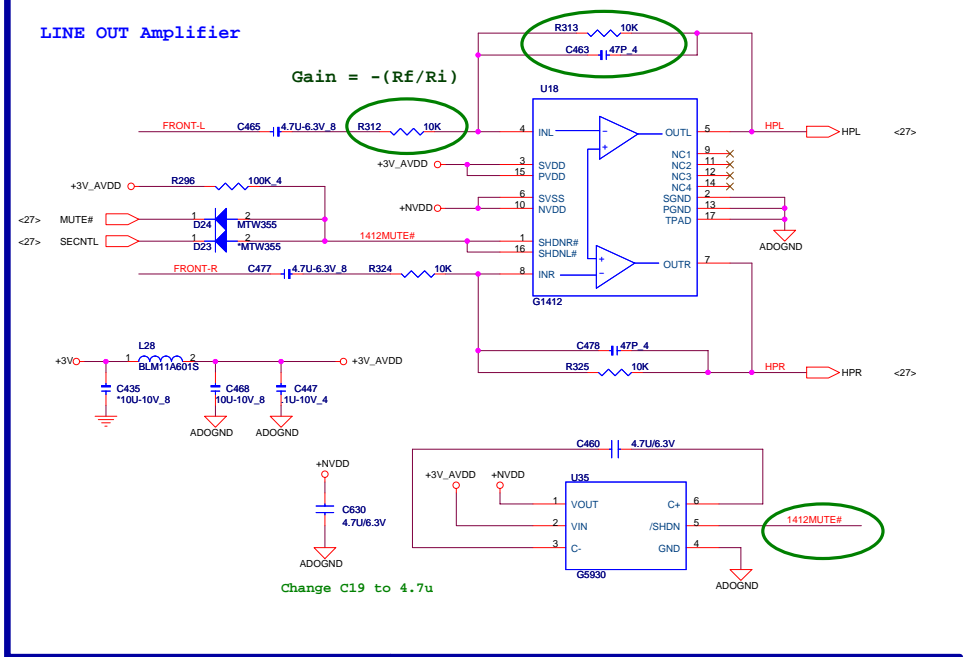
HOLES



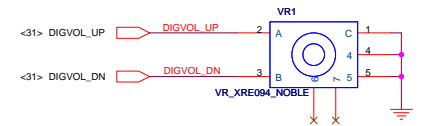
CODEC (ALC268)



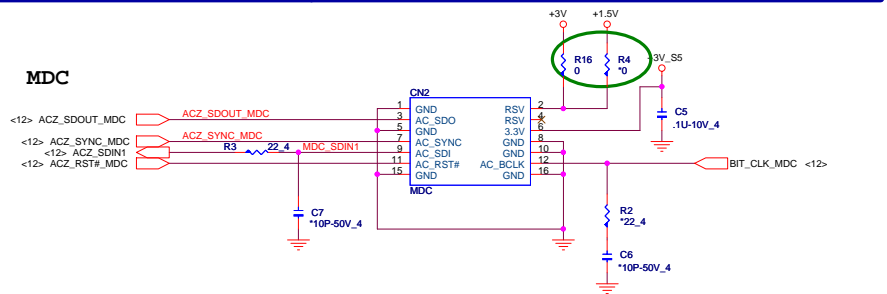
LINE OUT Amplifier




VR



MDC

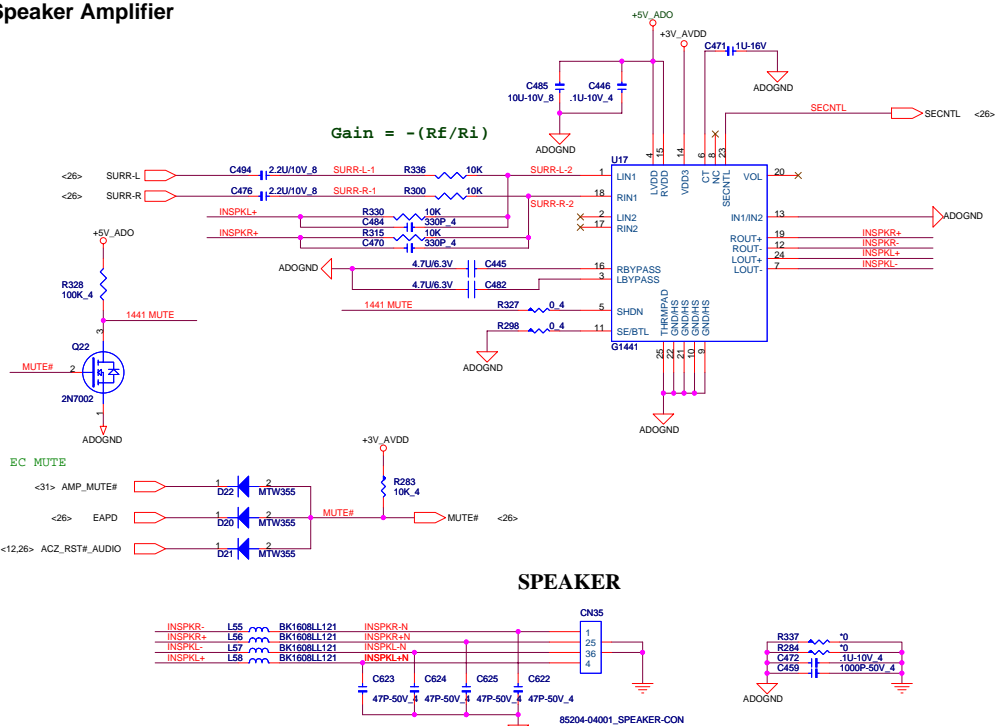




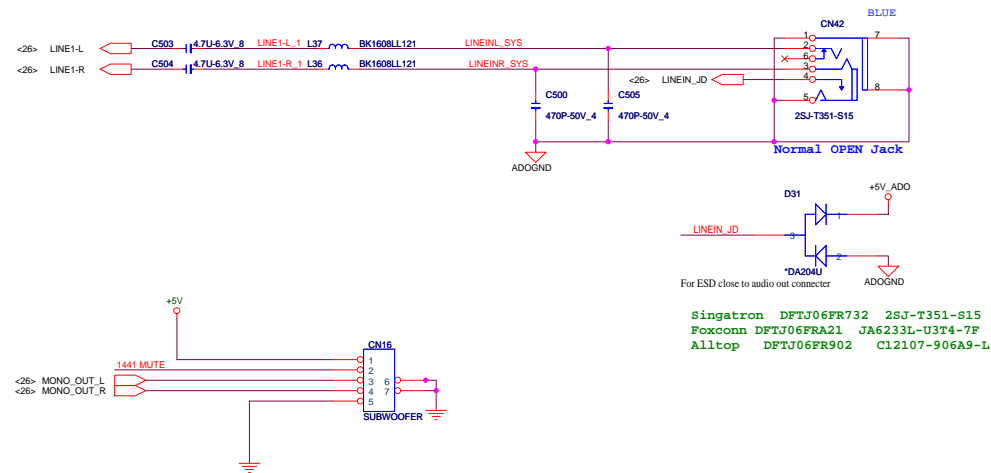
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Quanta Computer Inc.

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	REALTEK ALC268&888/MDC/VR		
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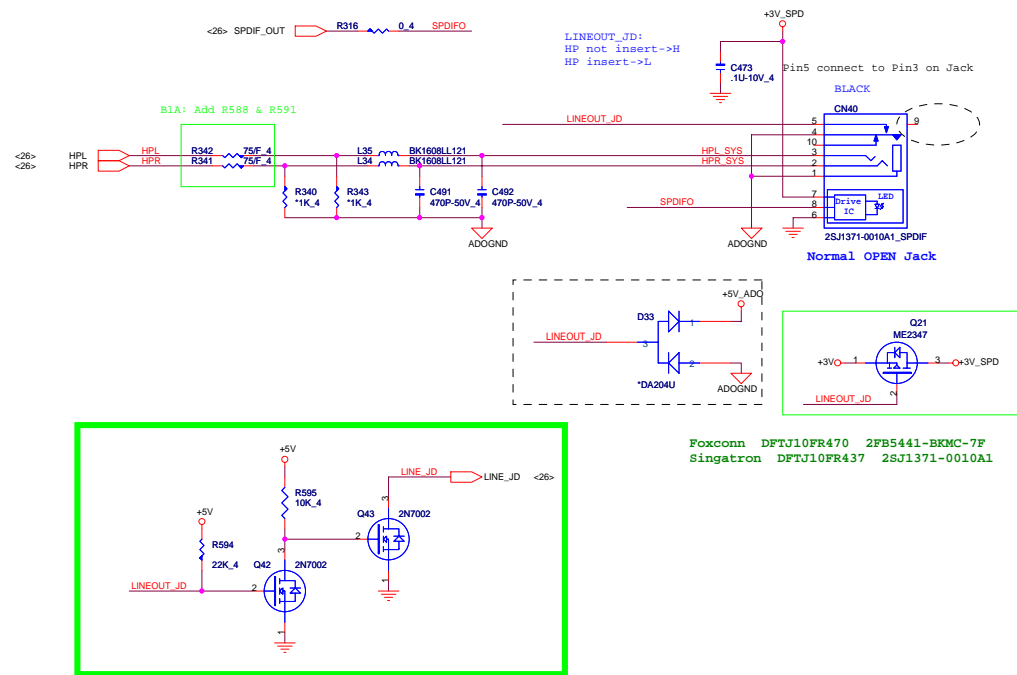
Speaker Amplifier



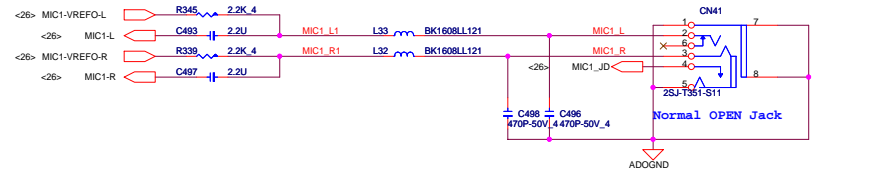
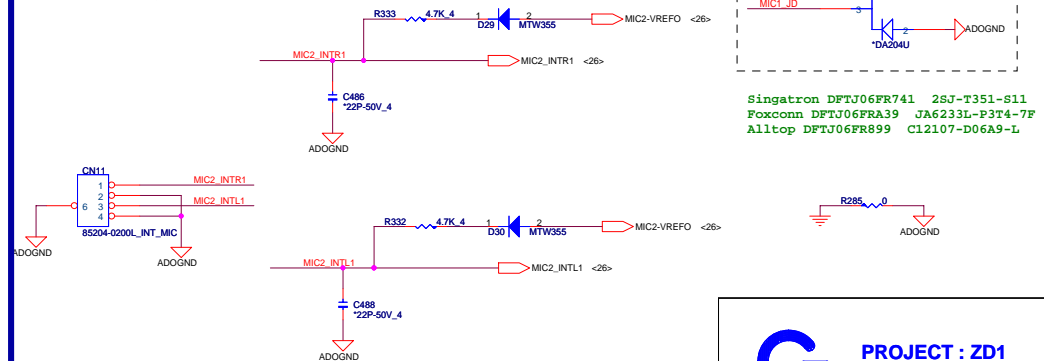
SYSTEM LINE IN/SUBWOOFER

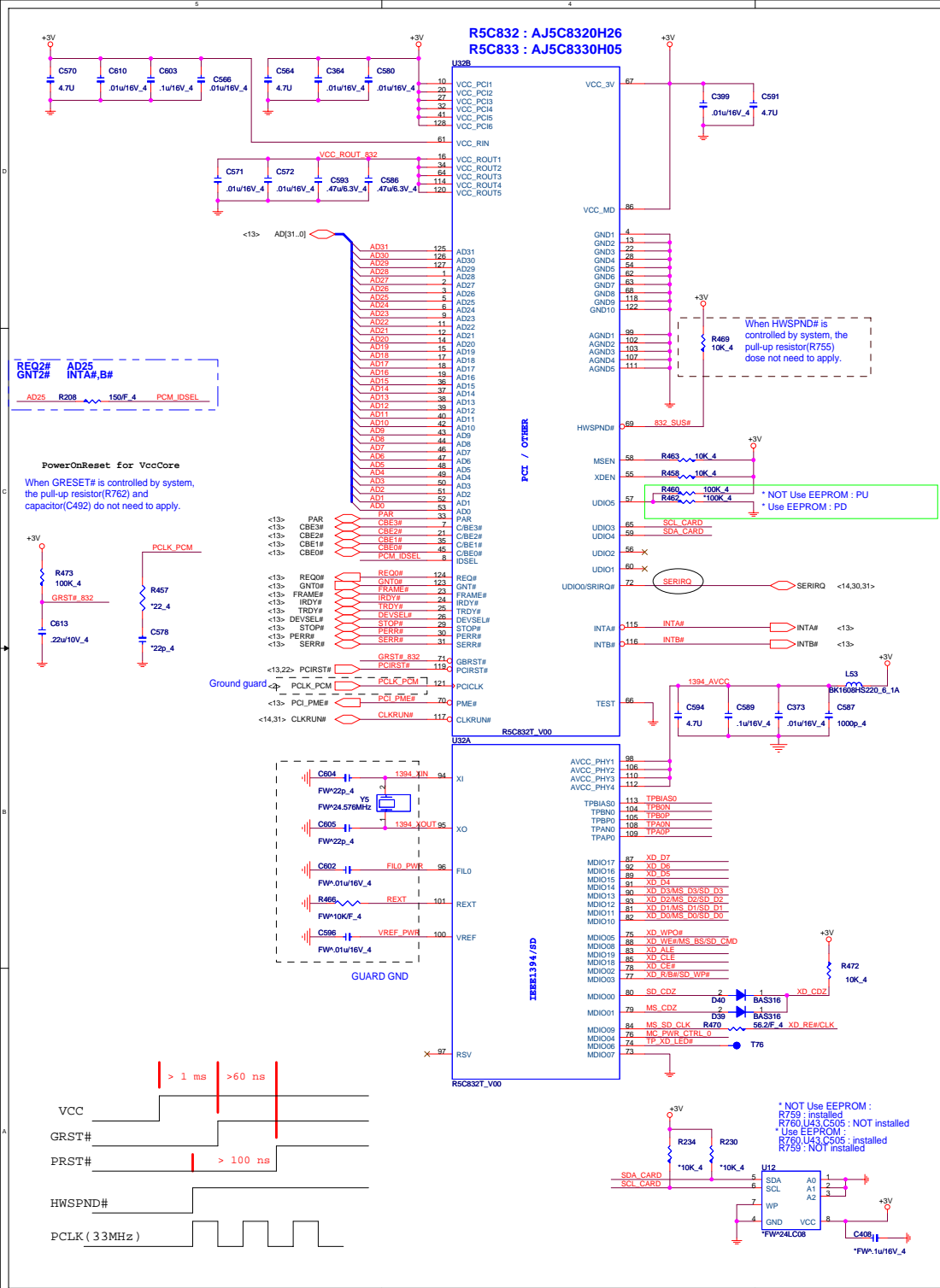


SYSTEM LINE OUT/SPDIF

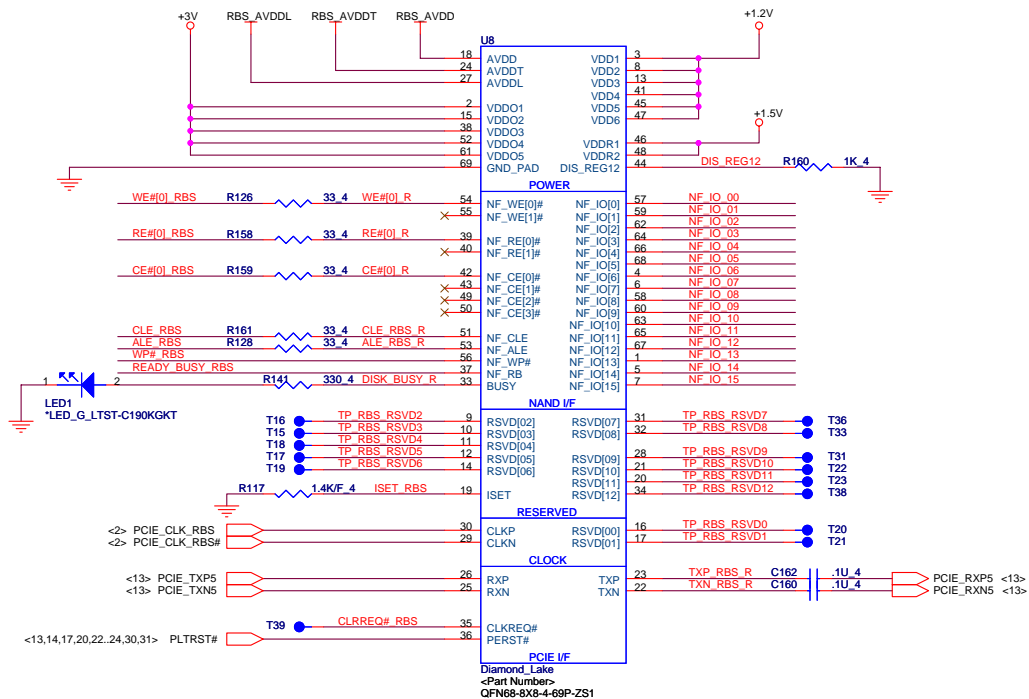


MIC

**INT MIC array**

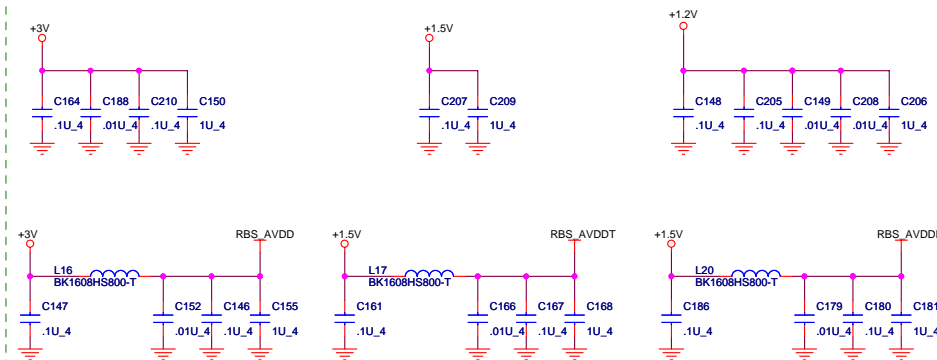


DIAMOND-LAKE ASIC



PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

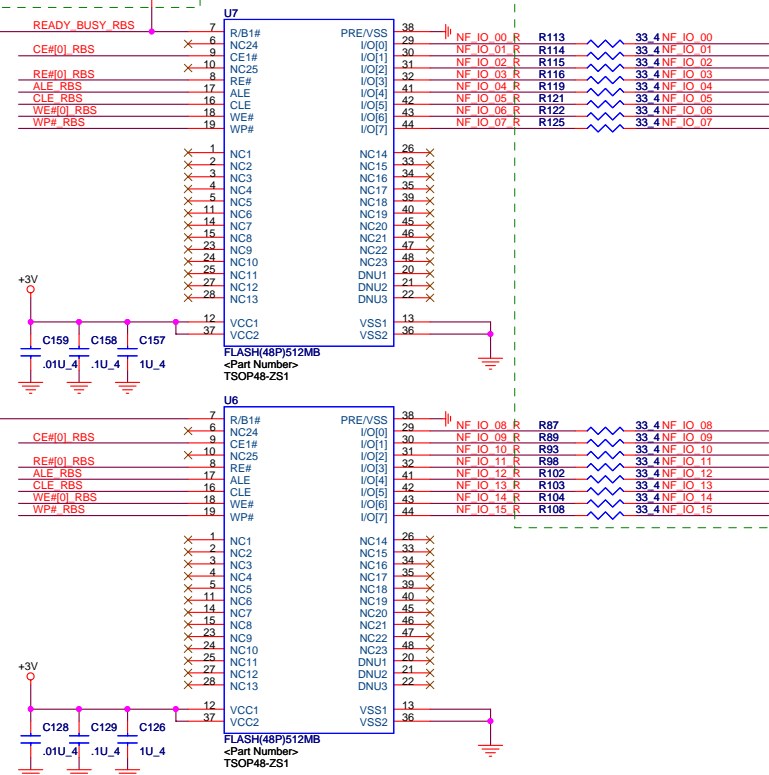
STUFF: INDICATES A 2KB VIRTUAL PAGE. => 256MB
DESTUFF: INDICATES A 4KB VIRTUAL PAGE => 512MB & 1024MB



PLACE CLOSE TO NAND FLASH

INTEL NAND FLASH

PLACEMENT NOTE:
PLACE TERMINATION RESISTORS
AT 10% TO 25% DISTANCE FROM
NAND FLASH.

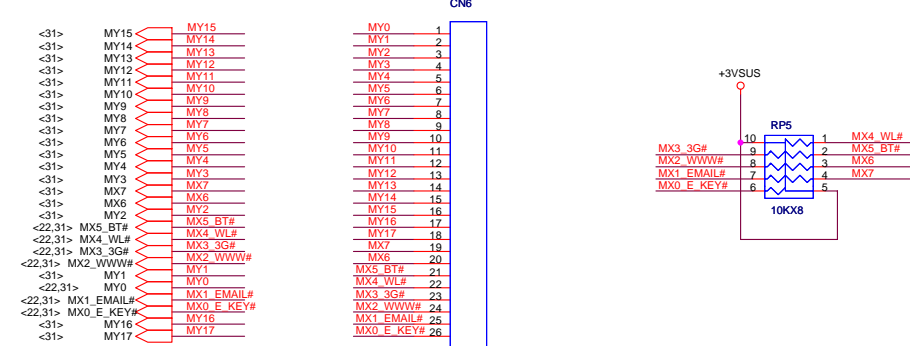


LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH
NEEDS TO HAVE A SOLDERMASK ON IT.



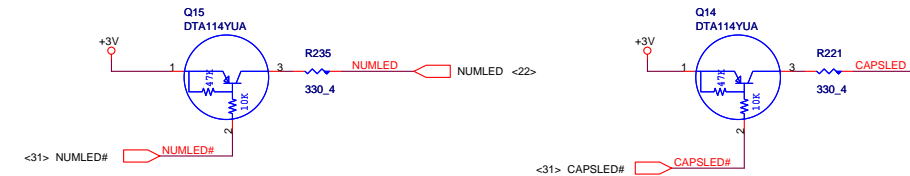
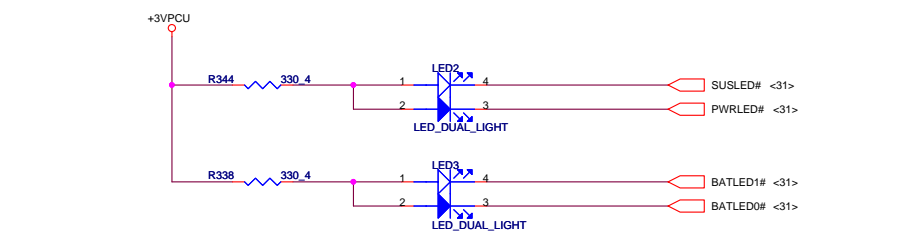
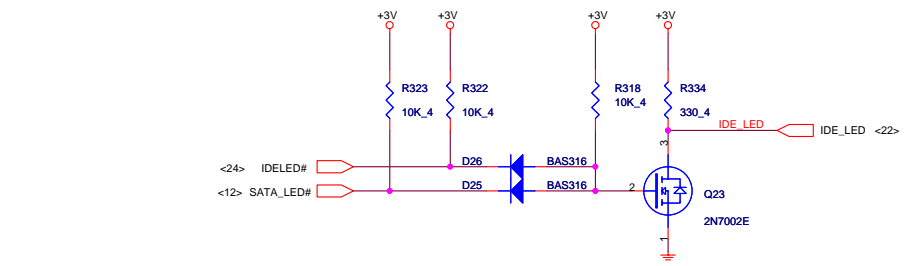
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Quanta Computer Inc.

INT K/B

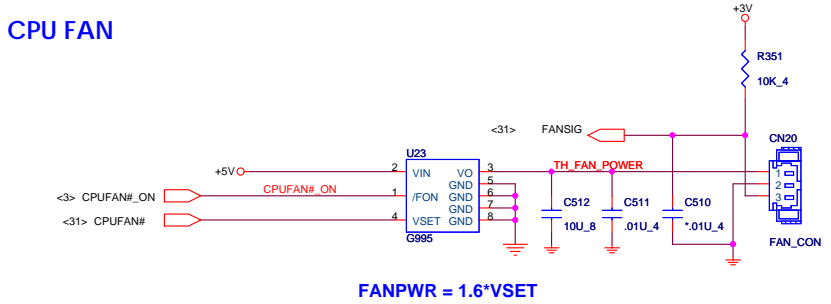


Acres 88502-2641

LED

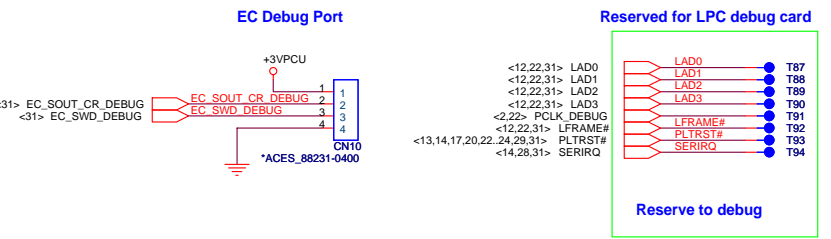


CPU FAN

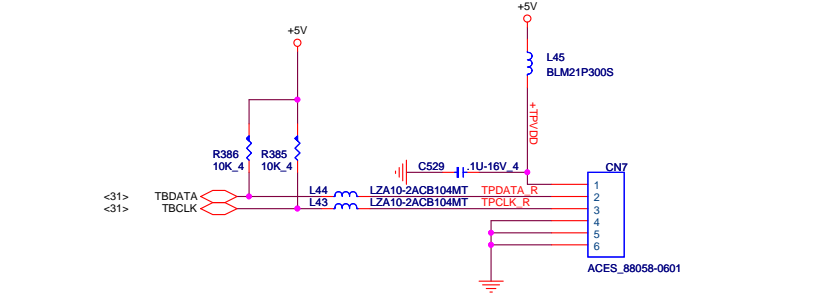


FANPWR = 1.6*VSET

DEBUG PORT



T/P



Size

Document Number

Date

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FAN,LED,KB,DEBUG PORT,TP

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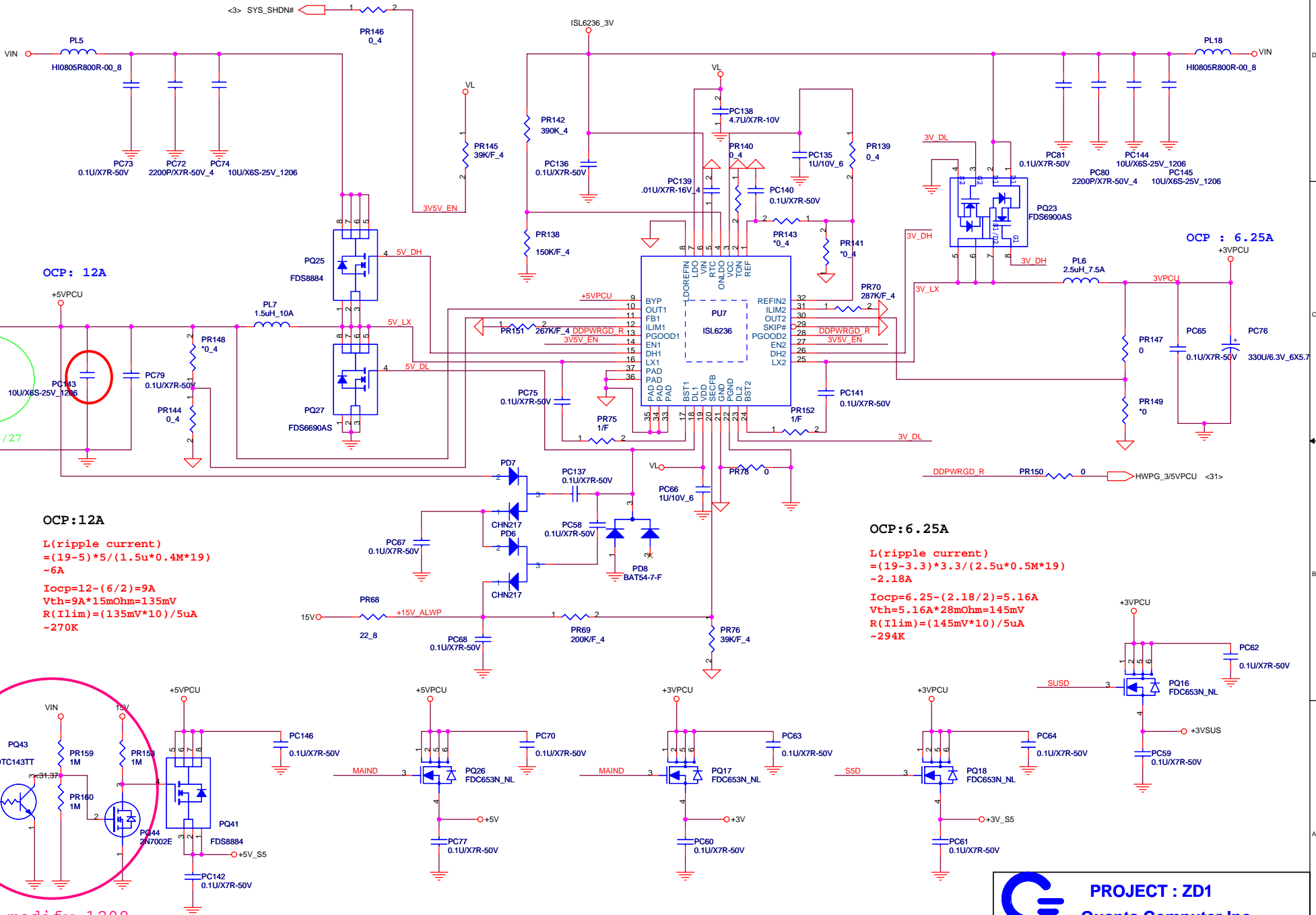
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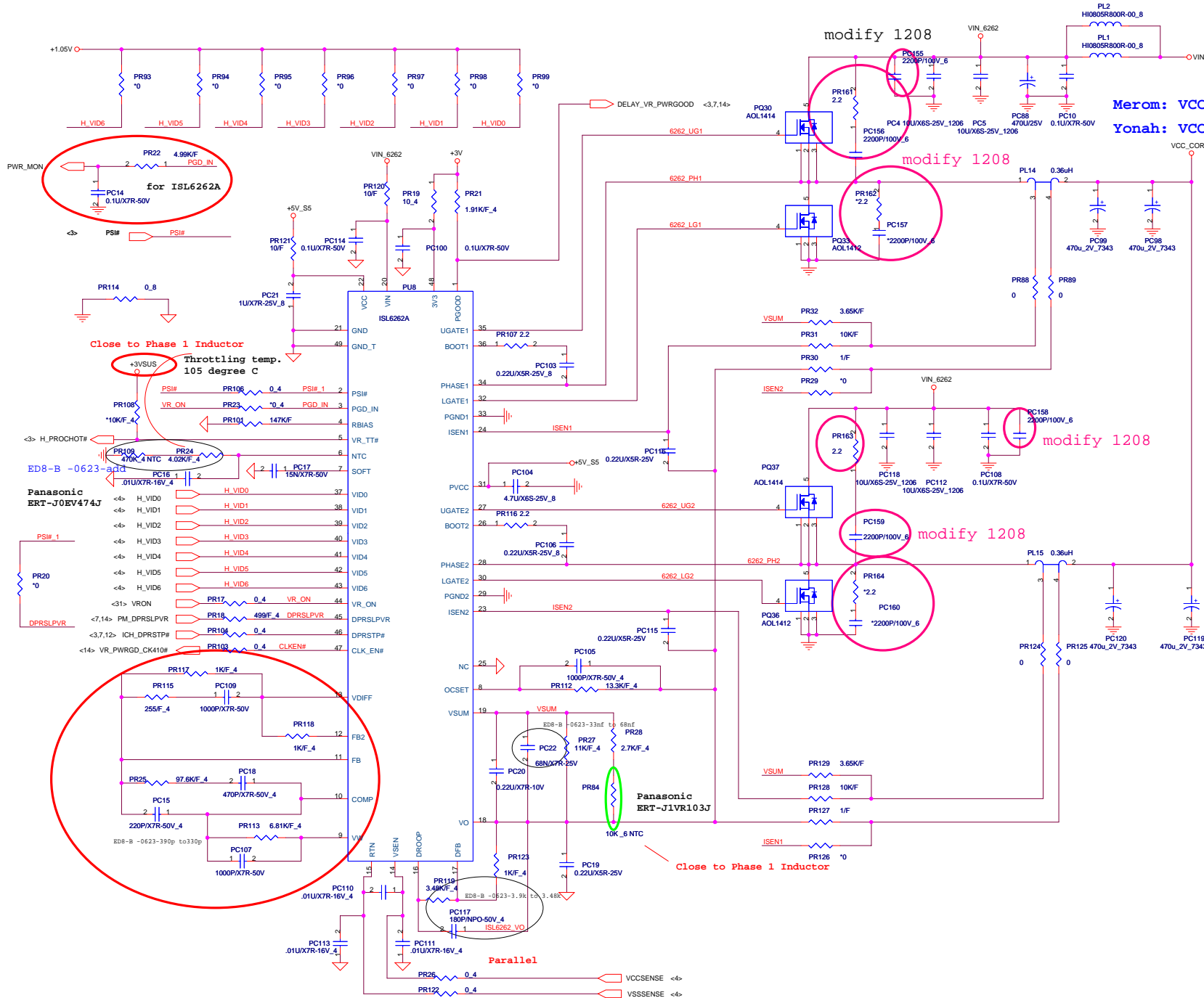
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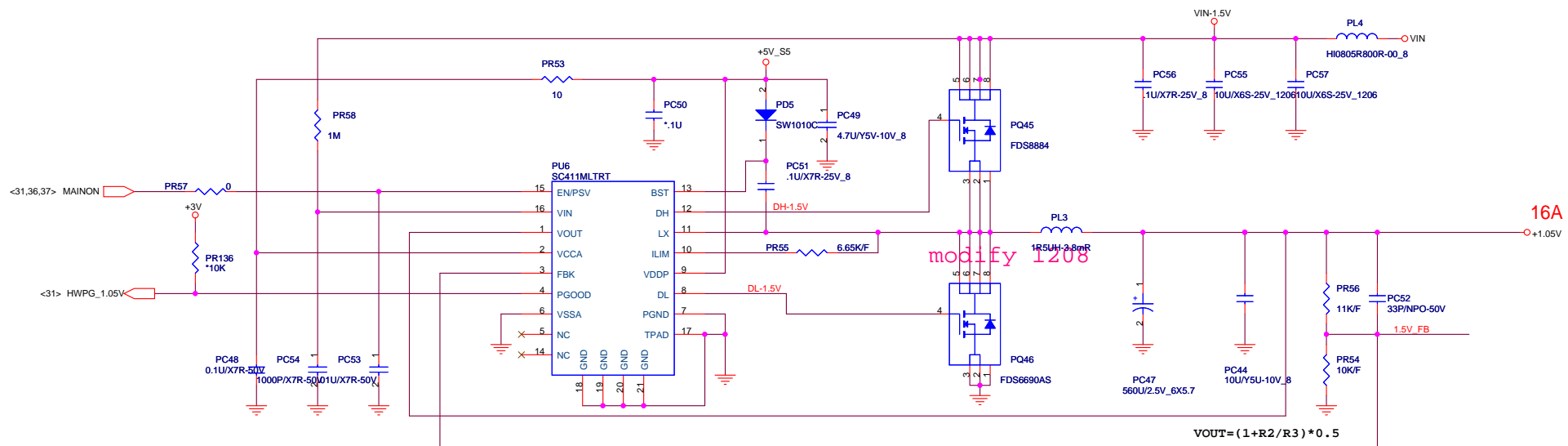
38

MAIND <36,37>
SUSD <37>



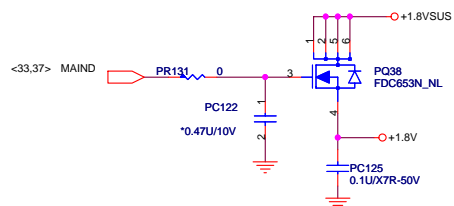
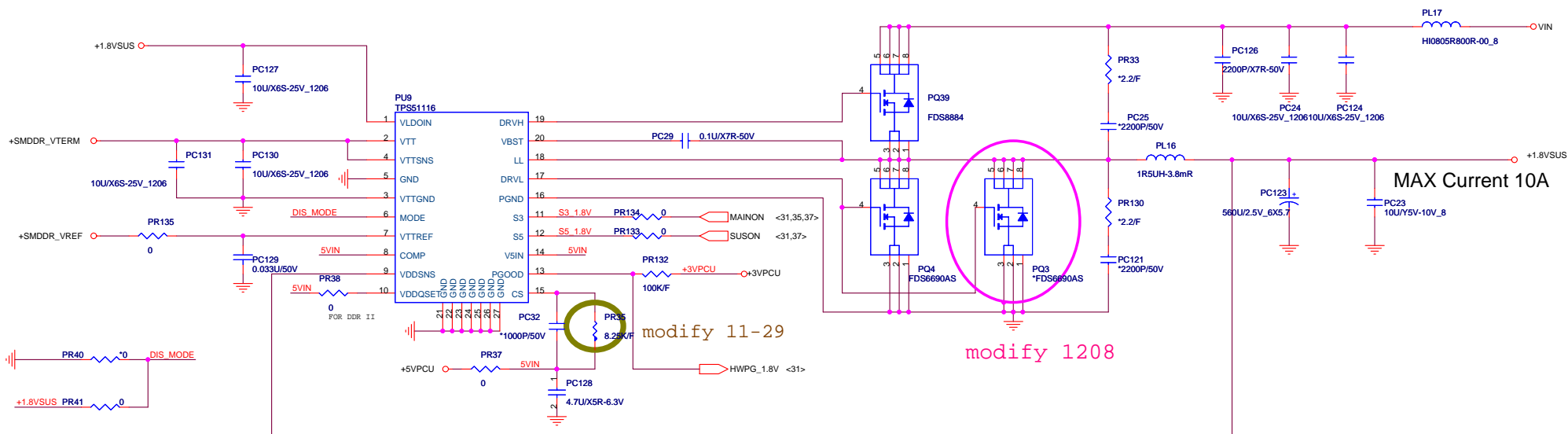


Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A




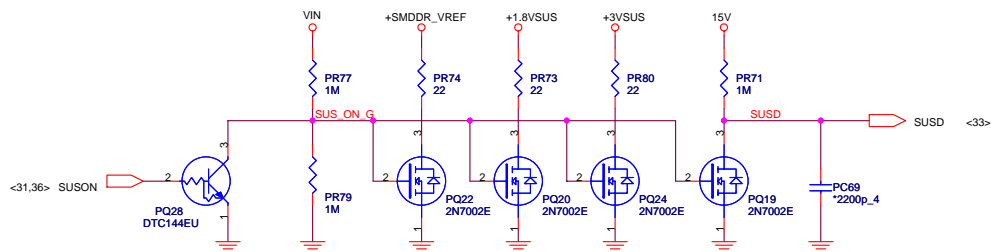
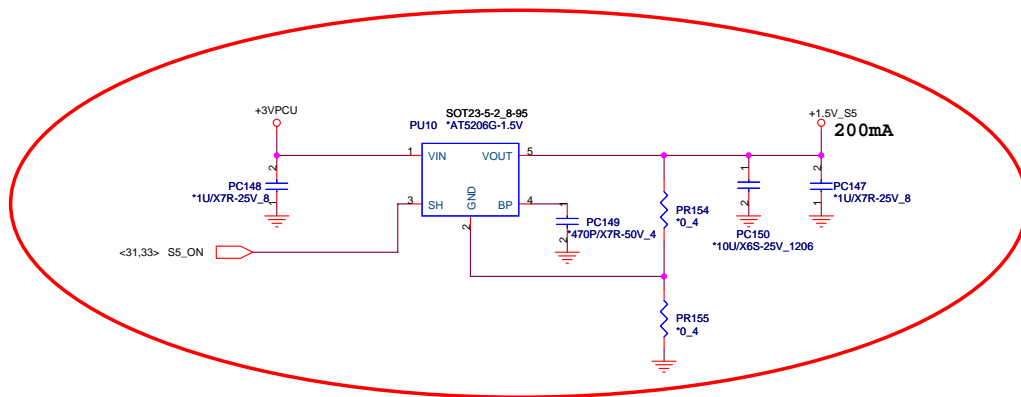
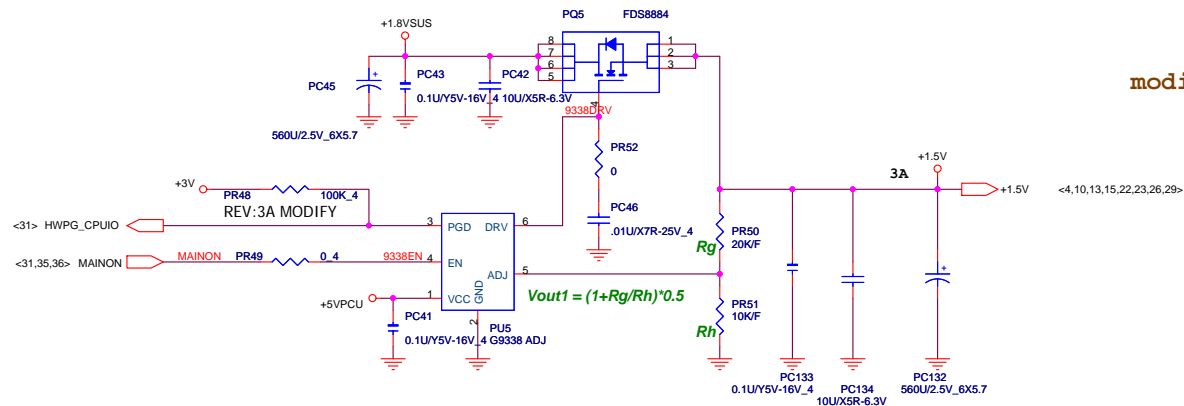
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	+1.5V / +2.5V	B
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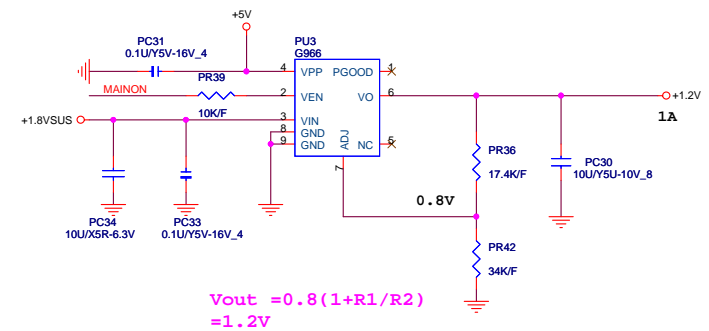
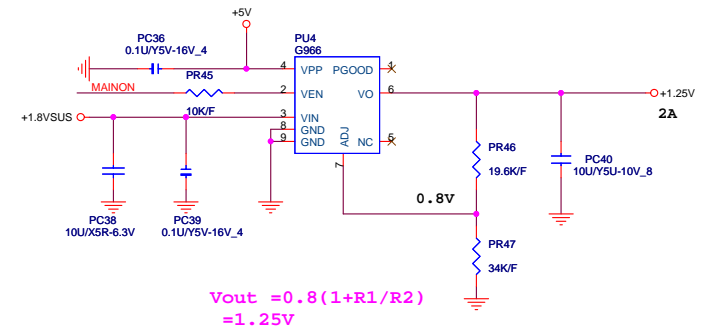
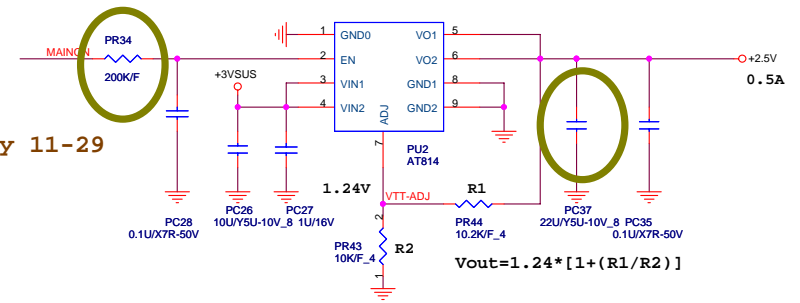


MAX Current 3.5A

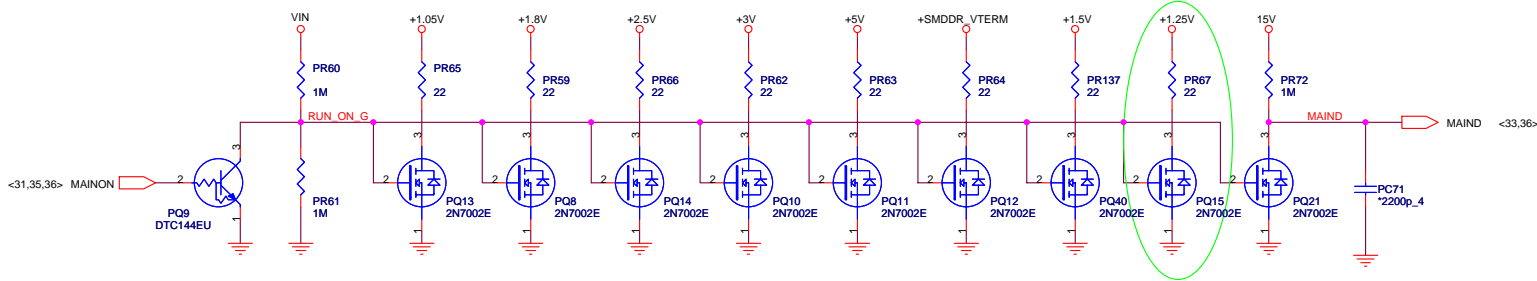
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modify 11-29



Add by power on 10/19



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